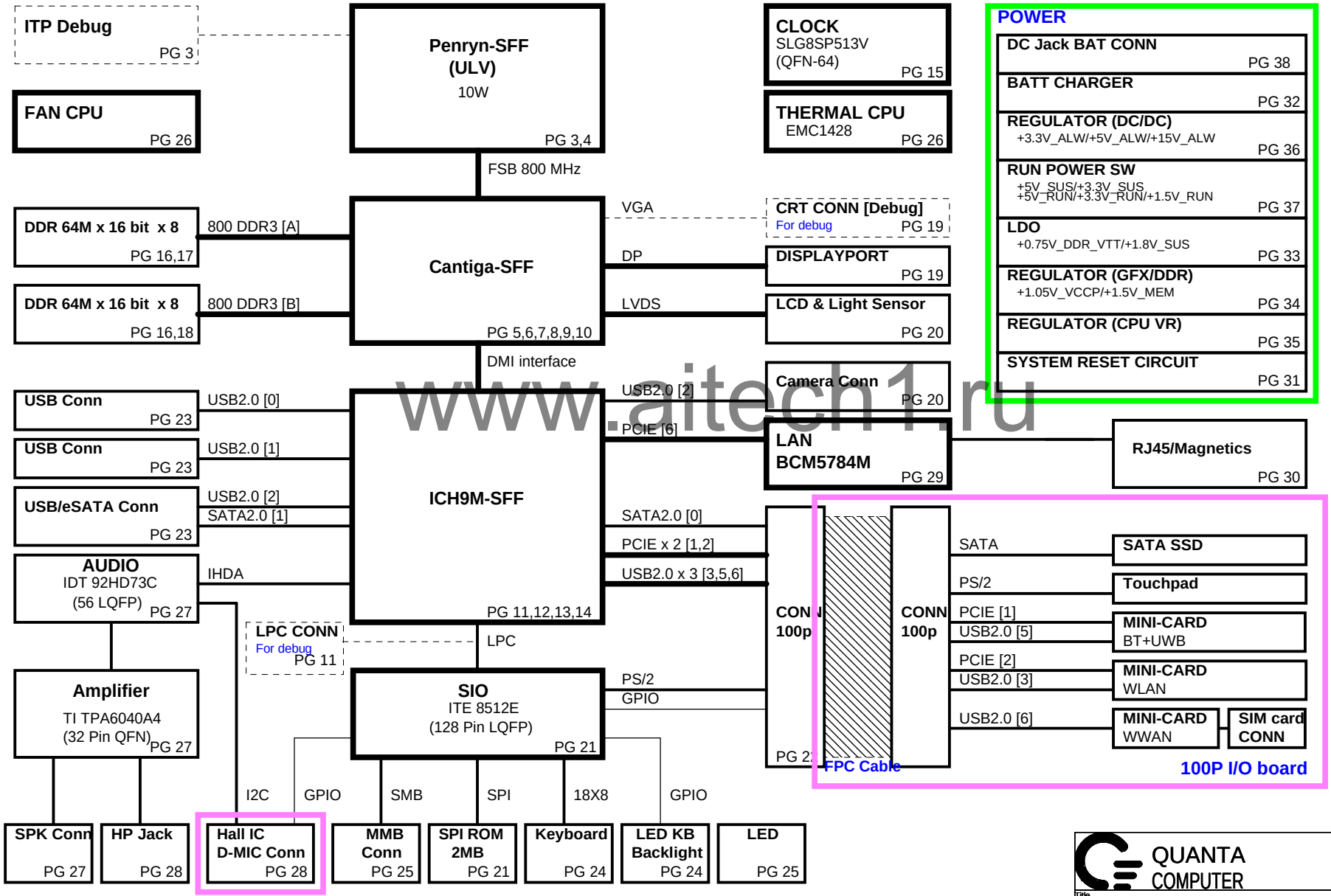
Adamo Montevina SFF Block Diagram

Rev: A00



QUANTA COMPUTER

Title	Schematic Block Diagram1	
Size	Document Number: SS5	Rev: 1A
Date: Tuesday, January 06, 2009	Sheet 1 of 44	

QUANTA COMPUTER

Title	Index & Power Status	
Size	Document Number: SS5	Rev: 1A
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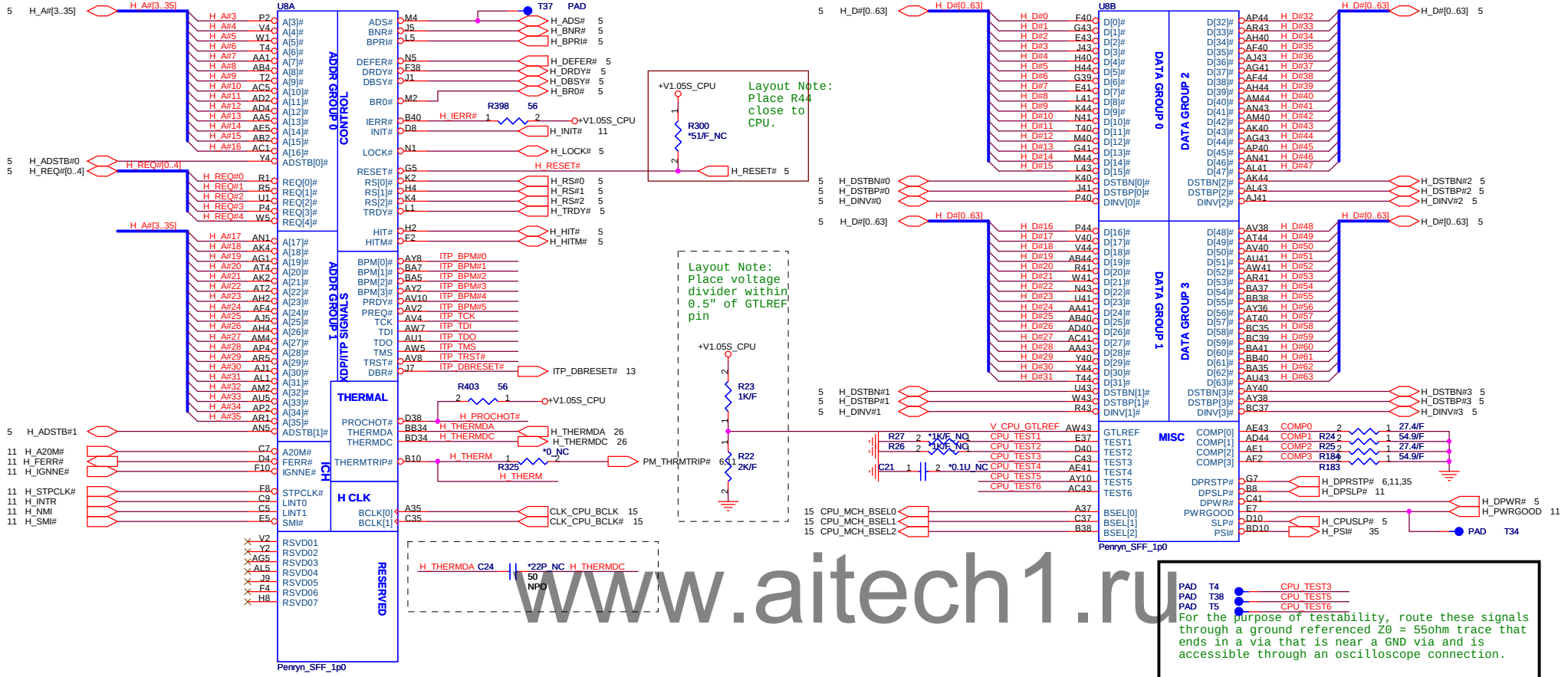
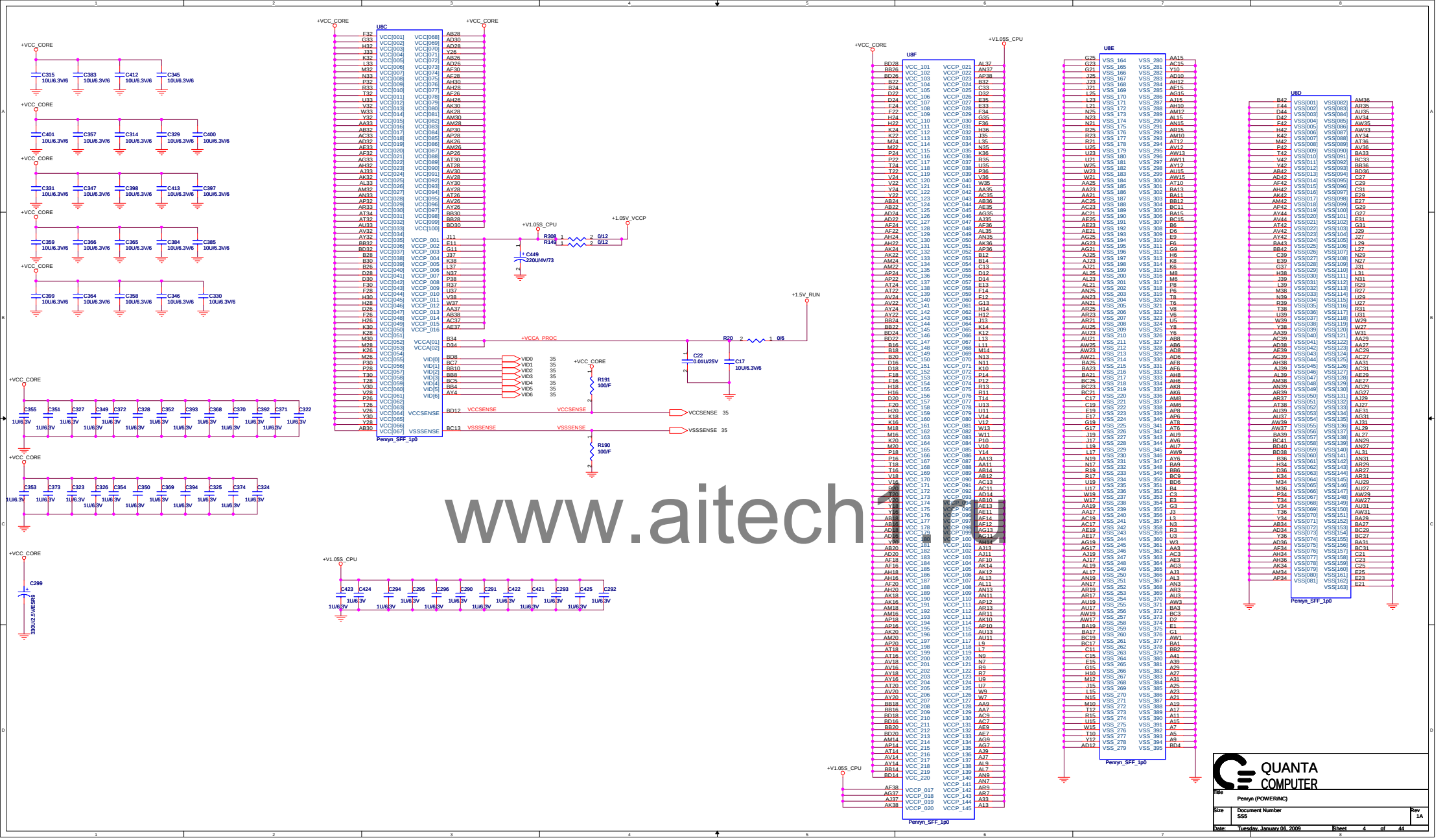
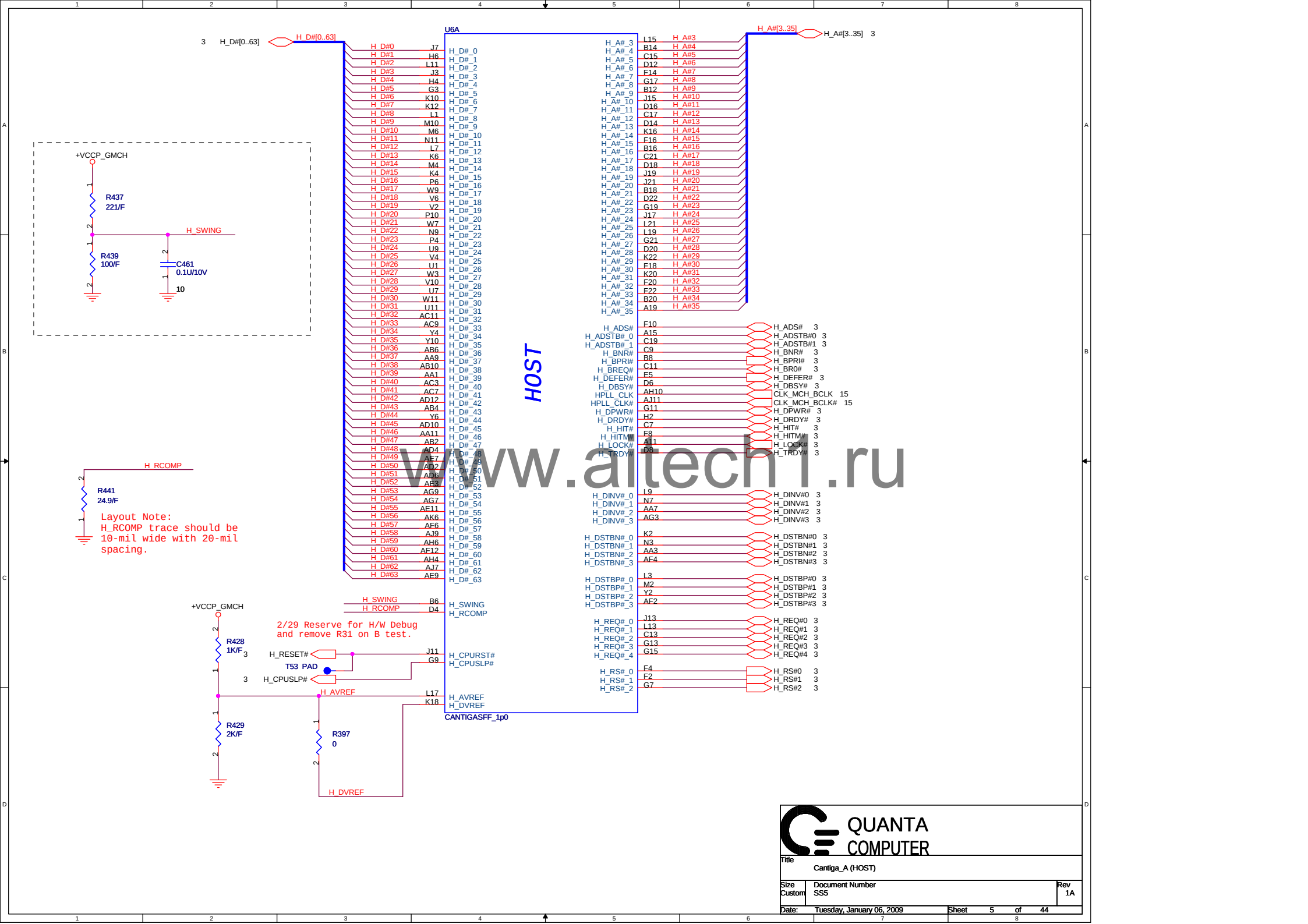
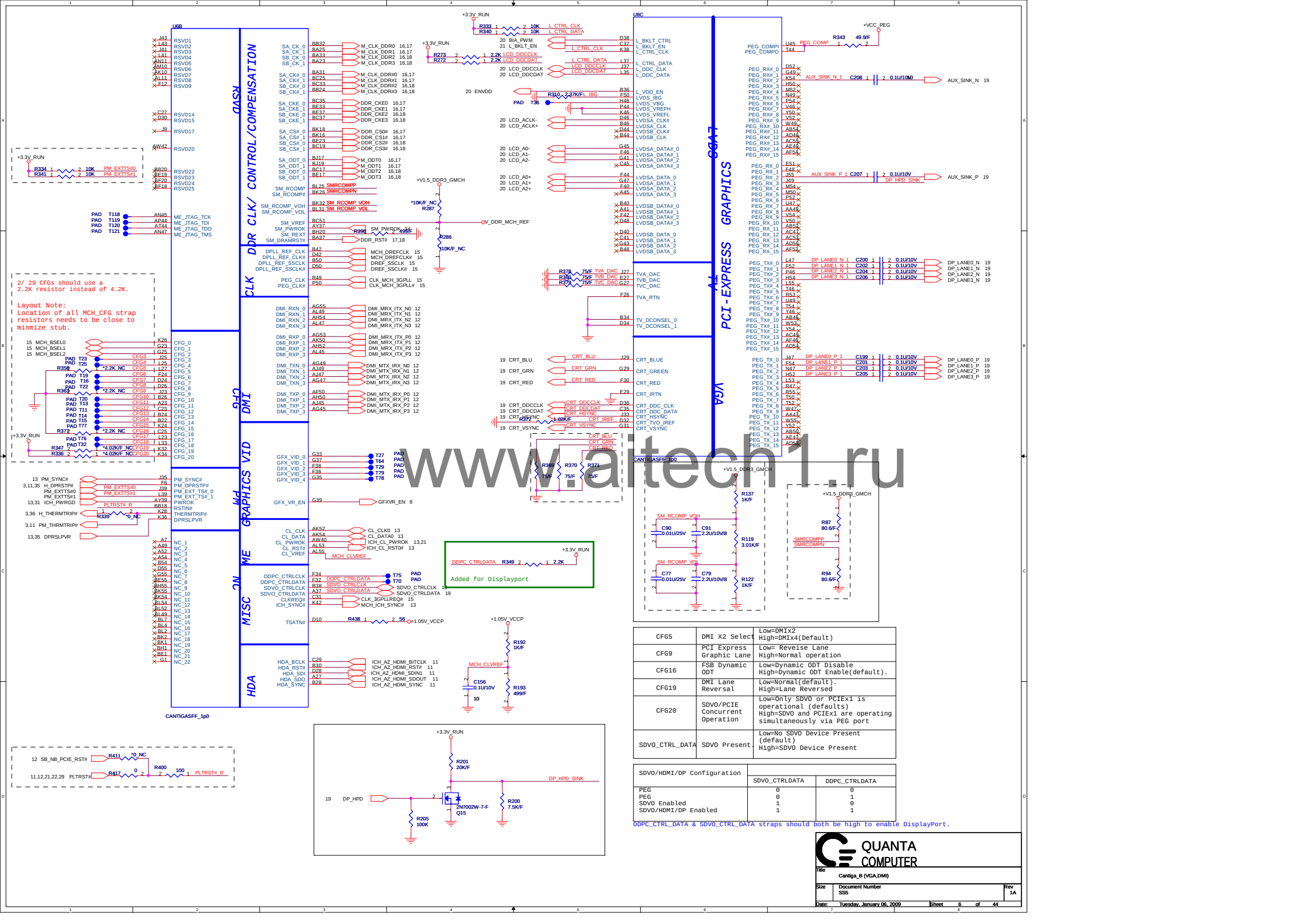

U8A
U8B
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
RESERVED
DATA GROUP 0
DATA GROUP 1
DATA GROUP 2
DATA GROUP 3
MISC
Penryn_SFF_1p0
Layout Note: Place R44 close to CPU.
Layout Note: Place voltage divider within 0.5" of GTLREF pin
www.aitech1.ru
For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.
Populate ITP700Flex for bringup
Layout Note: Place couple 0.1uF Decoupling caps with in 0.1" ITP connector.
*CONN_ITP700Flex_NC
Voltage Level shift
Signal | ITP disable guidelines
TDI | Resistor Value
TMS | 150 ohm +/- 5% | Connect To | Resistor Placement
TRST# | 39 ohm +/- 5% | VTT | Within 2.0" of the ITP
TCK | 680 ohm +/- 5% | VTT | Within 2.0" of the ITP
TDO | 27 ohm +/- 5% | Open GND | Within 2.0" of the ITP
ITP_EN | | GND | Within 2.0" of the ITP
R268 Depop | | VTT | Within 2.0" of the ITP
+3VRUN | Close to CK410M Pin8
QUANTA COMPUTER
Title: Penryn (HOST BUS)
Size | Document Number: SS5 | Rev: 1A
Date: Tuesday, January 06, 2009 | Sheet 3 of 44


U8C
U8F
U8E
U8D
+VCC_CORE
+V1.05S_CPU
+1.05V_VCCP
+1.5V_RUN
+VCCA_PROC
VCCSENSE
VSSSENSE
R308 0/12
R148 0/12
+C449 220U/4V/73
C22 0.01U/25V
C17 10U/6.3V/6
R20 0/6
R191 100/F
R190 100/F
Penryn_SFF_1p0
QUANTA COMPUTER
Title
Penryn (POWER/NC)
Size
Document Number
SS5
Rev
1A
Date: Tuesday, January 06, 2009
Sheet 4 of 44



QUANTA COMPUTER

Title	Cantiga_A (HOST)		
Size: Custom	Document Number: SS5		Rev: 1A
Date: Tuesday, January 06, 2009	Sheet 5 of 44		



CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low= Reveise Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating simultaneously via PEG port
SDVO_CTRL_DATA	SDVO Present.	Low=No SDVO Device Present (default) High=SDVO Device Present

SDVO/HDMI/DP Configuration		
	SDVO_CTRLDATA	DDPC_CTRLDATA
PEG	0	0
PEG	0	1
SDVO Enabled	1	0
SDVO/HDMI/DP Enabled	1	1

Title	Cantiga_B (VGA,DMI)
Size	SS5
Document Number	
Rev	1A
Date:	Tuesday, January 06, 2009
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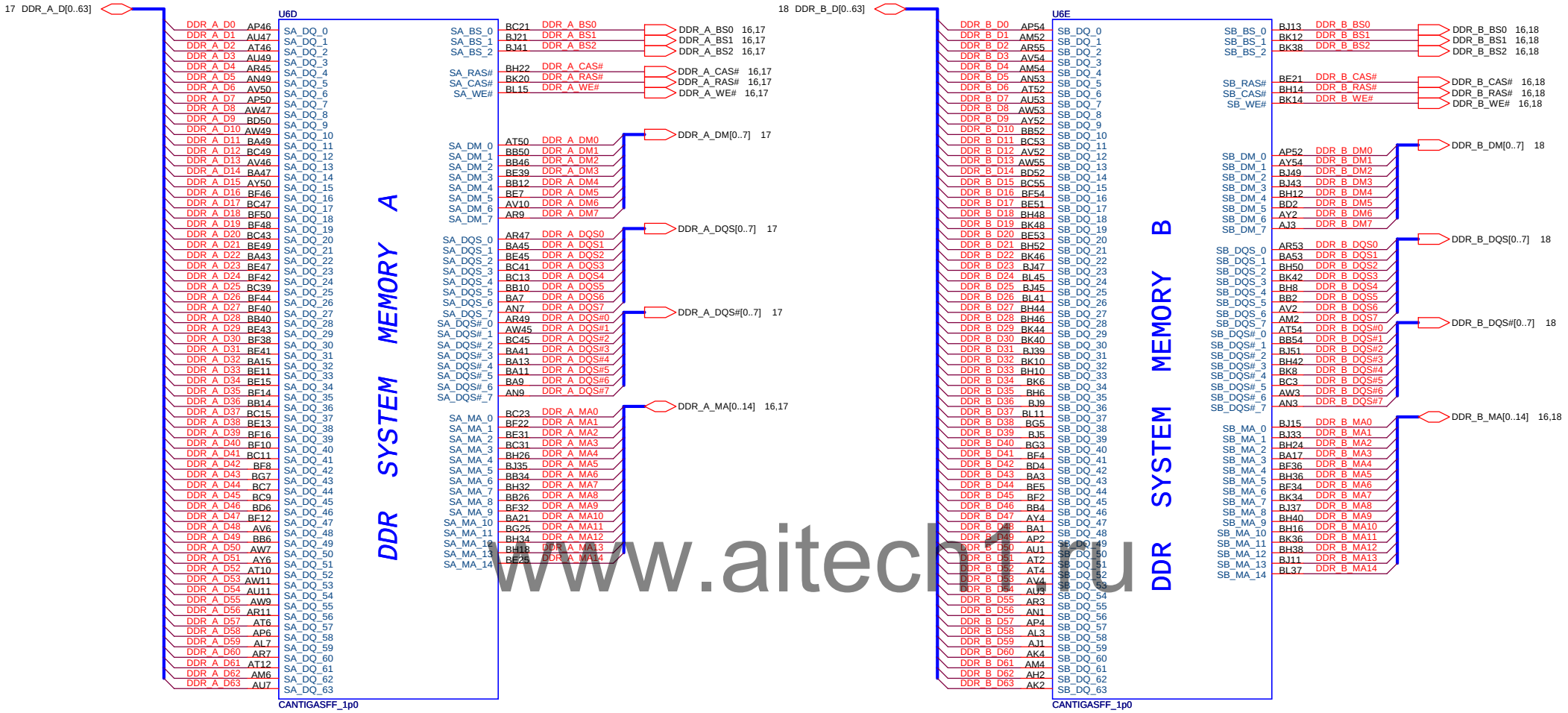
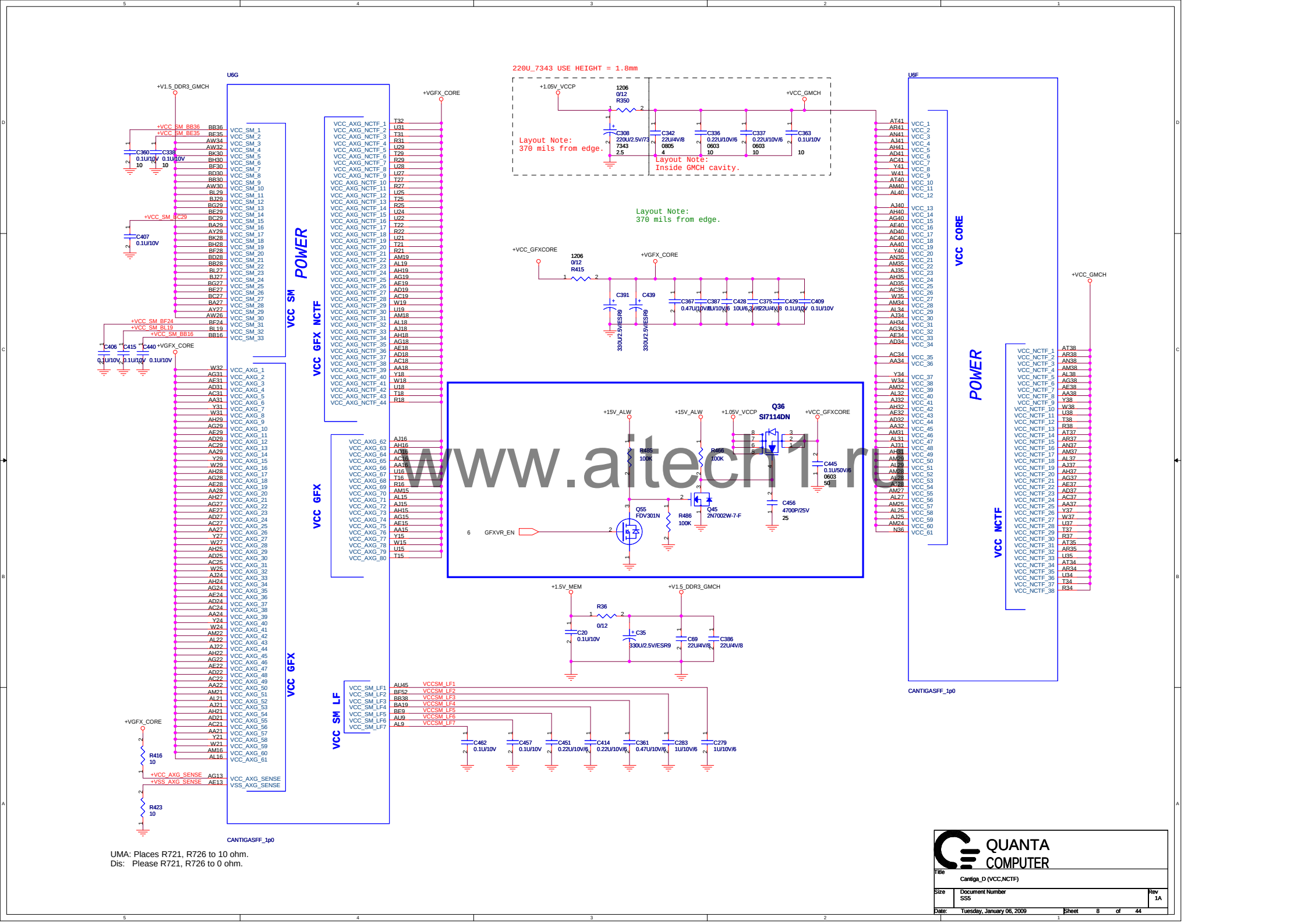
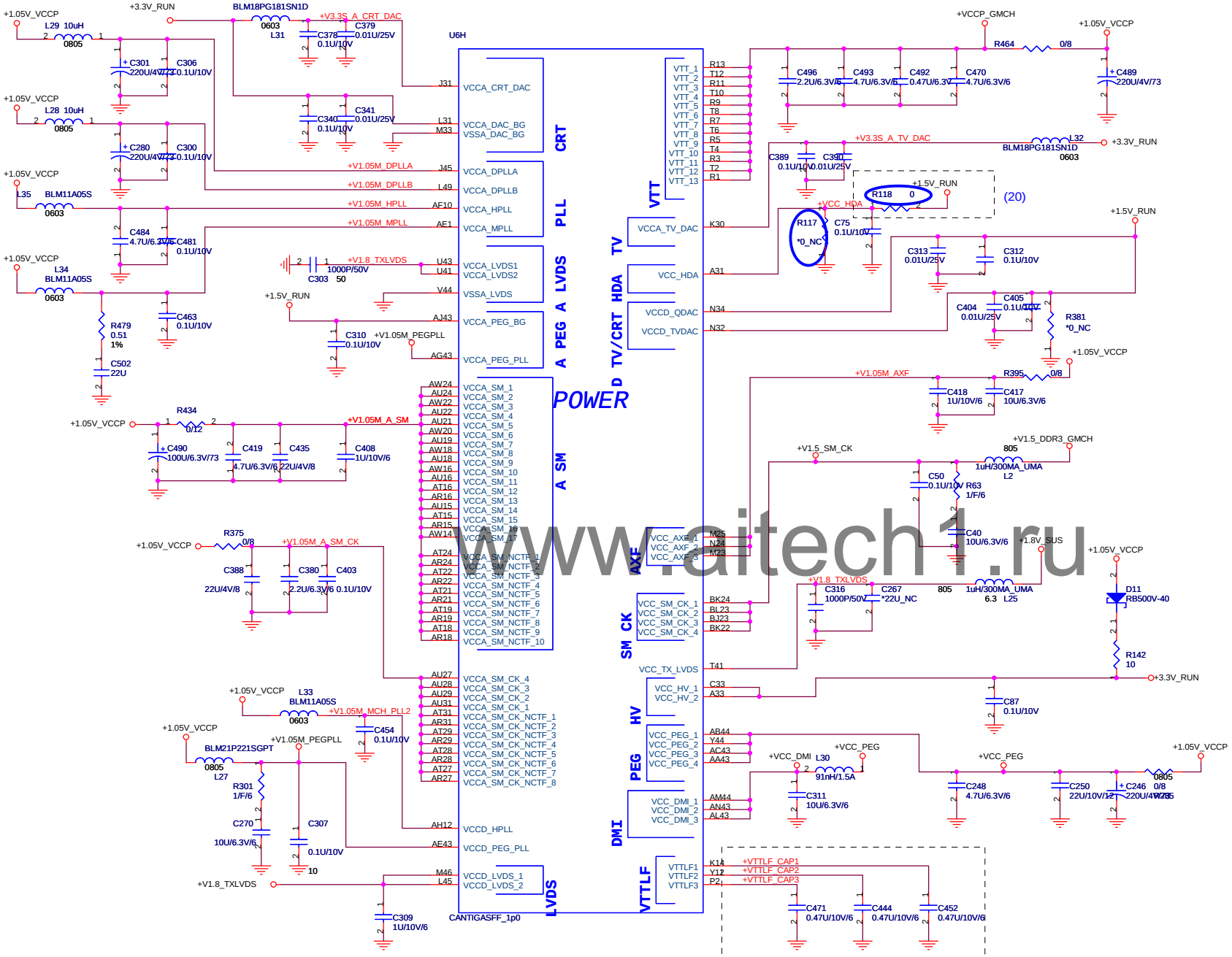


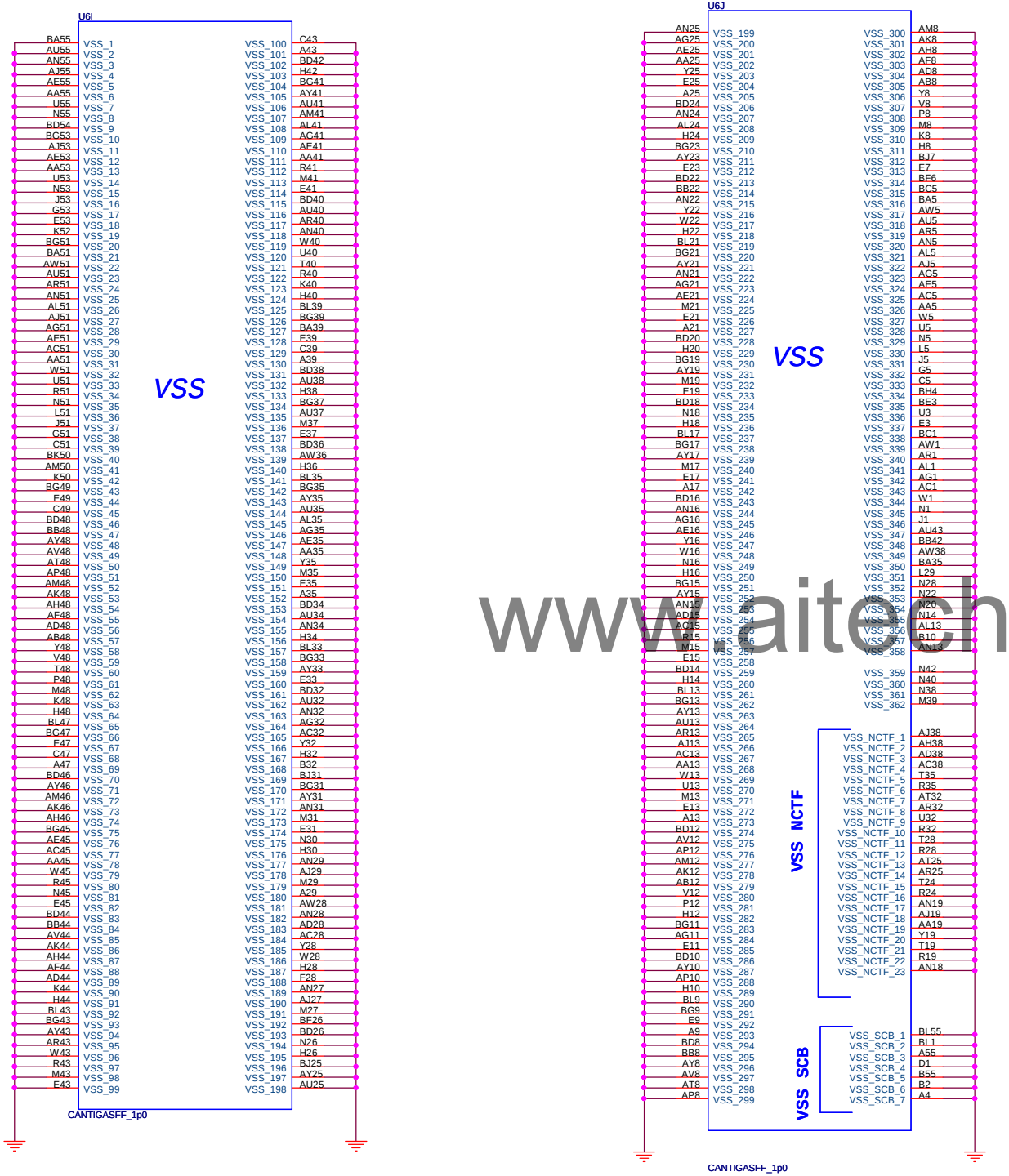
QUANTA COMPUTER

Title	Cantiga_C (DDR3)	
Size	Document Number SS5	Rev 1A
Date: Tuesday, January 06, 2009	Sheet 7 of 44	



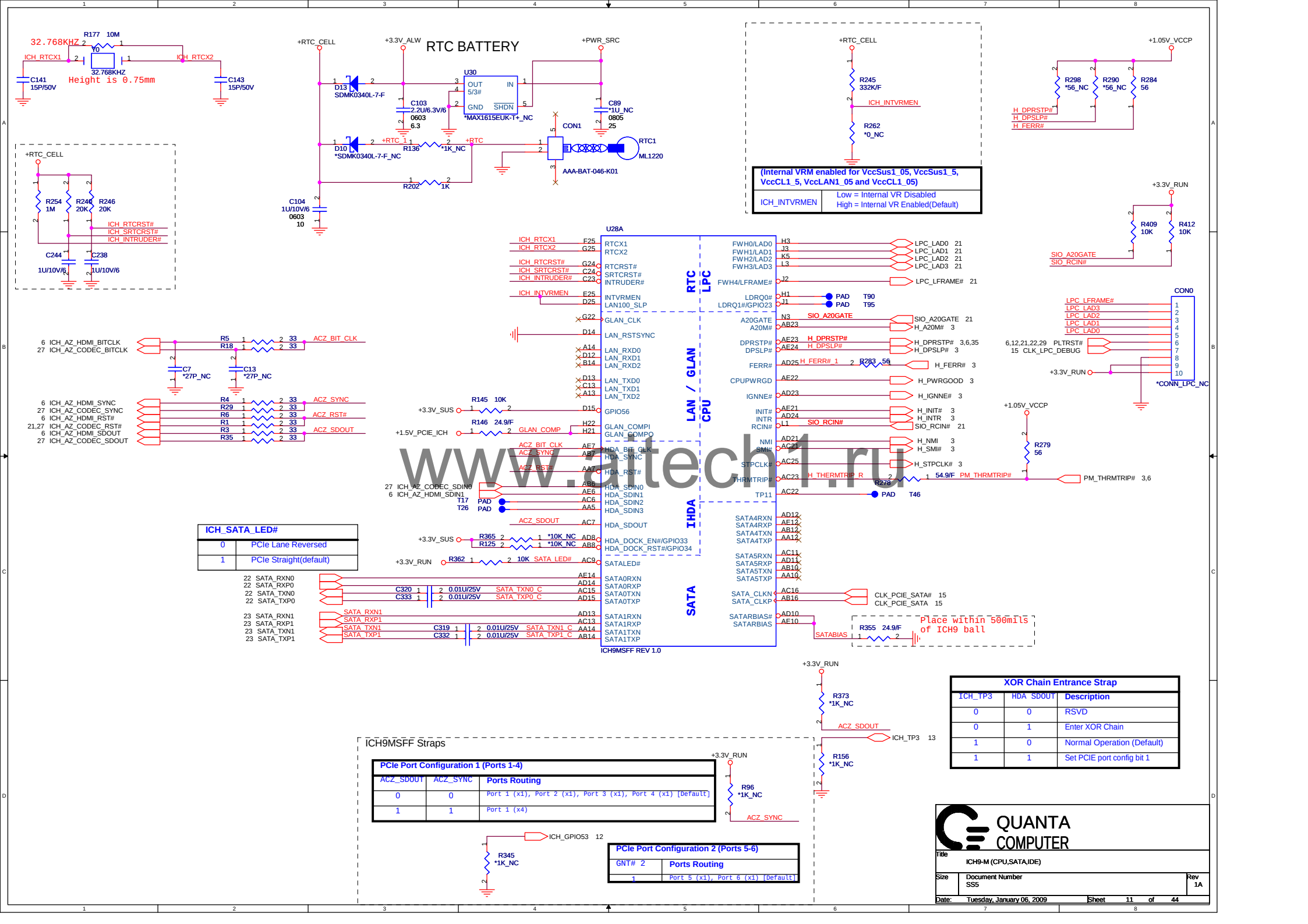


QUANTA COMPUTER		
Title	Cantiga_E (POWER)	
Size	Document Number SS5	Rev 1A
Date: Tuesday, January 06, 2009	Sheet 9 of 44	



QUANTA COMPUTER

Title	Cantiga_F (VSS)		
Size	Document Number SS5		Rev 1A
Date:	Tuesday, January 06, 2009	Sheet 10 of 44	



Place TX DC blocking caps close ICH9.

BT & UWB

22 PCIE_RX1-
22 PCIE_RX1+
22 PCIE_TX1-
22 PCIE_TX1+

C119 1 2 0.1U/10V
C113 1 2 0.1U/10V

PCIE_TXN1_C
PCIE_TXP1_C

WLAN

22 PCIE_RX2-
22 PCIE_RX2+
22 PCIE_TX2-
22 PCIE_TX2+

C115 1 2 0.1U/10V
C114 1 2 0.1U/10V

PCIE_TXN2_C
PCIE_TXP2_C

U28D

PCI-Express

PERN1 T25
PERP1 T24
PETN1 R24
PETP1 R23

PERN2 P25
PERP2 P24
PETN2 P21
PETP2 P22

PERN3 N23
PERP3 N24
PETN3 M21
PETP3 M22

PERN4 M25
PERP4 M24
PETN4 L24
PETP4 L23

PERN5 K24
PERP5 K25
PETN5 K21
PETP5 K22

Direct Media Interface

DMI0RXN V25
DMI0RXP V24
DMI0TXN U24
DMI0TXP U23

DMI1RXN W23
DMI1RXP W24
DMI1TXN V21
DMI1TXP V22

DMI2RXN Y24
DMI2RXP Y25
DMI2TXN Y21
DMI2TXP Y22

DMI3RXN AB24
DMI3RXP AB25
DMI3TXN AA23
DMI3TXP AA24

DMI_CLKN T21
DMI_CLKP T22

DMI_ZCOMP AB21
DMI_IRCOMP AB22 DMI_COMP

DMI_MTX_IRX_N0 6
DMI_MTX_IRX_P0 6
DMI_MRX_ITX_N0 6
DMI_MRX_ITX_P0 6

DMI_MTX_IRX_N1 6
DMI_MTX_IRX_P1 6
DMI_MRX_ITX_N1 6
DMI_MRX_ITX_P1 6

DMI_MTX_IRX_N2 6
DMI_MTX_IRX_P2 6
DMI_MRX_ITX_N2 6
DMI_MRX_ITX_P2 6

DMI_MTX_IRX_N3 6
DMI_MTX_IRX_P3 6
DMI_MRX_ITX_N3 6
DMI_MRX_ITX_P3 6

CLK_PCIE_ICH# 15
CLK_PCIE_ICH 15

R162 24.9/F
+1.5V_PCIE_ICH

Place within 500mils of ICH9

For EA test use

ET0 1 PCIE_RX1+
ET5 1 PCIE_RX2-

Giga Bit LOM

29 PCIE_RX6-/GLAN_RX-
29 PCIE_RX6+/GLAN_RX+
29 PCIE_TX6-/GLAN_TX-
29 PCIE_TX6+/GLAN_TX+

C117 1 2 0.1U/10V
C116 1 2 0.1U/10V

GLAN_TXN_C
GLAN_TXP_C

PERN6/GLAN_RXN H24
PERP6/GLAN_RXP H25
PETN6/GLAN_TXN J24
PETP6/GLAN_TXP J23

USB

USBP0N AE2
USBP0P AD1
USBP1N AD3
USBP1P AD4
USBP2N AC2
USBP2P AC3
USBP3N AC5
USBP3P AB4
USBP4N AB2
USBP4P AB1
USBP5N AA3
USBP5P AA2
USBP6N Y1
USBP6P Y2
USBP7N W2
USBP7P W3
USBP8N V1
USBP8P V2
USBP9N Y5
USBP9P Y4
USBP10N U3
USBP10P U2
USBP11N V4
USBP11P V5

ICH_USBP0- 23
ICH_USBP0+ 23
ICH_USBP1- 23
ICH_USBP1+ 23
ICH_USBP2- 23
ICH_USBP2+ 23
ICH_USBP3- 22
ICH_USBP3+ 22
ICH_USBP4- 20
ICH_USBP4+ 20
ICH_USBP5- 22
ICH_USBP5+ 22
ICH_USBP6- 22
ICH_USBP6+ 22

ICH_USBP2-
ICH_USBP2+
ICH_USBP3-
ICH_USBP3+

TO Daughter Board
TO Daughter Board
TO Daughter Board
WLAN
Camera
BT&UWB
WWAN

SPI

SPI_CLK E24
SPI_CS0# E23
SPI_CS1#/GPIO58/CLGPIO6 F23
SPI_MOSI F22
SPI_MISO G23

T49 PAD
T55 PAD
T35 PAD
T52 PAD

ICH_SPI_CS1# R

ICH_SPI_CS1# R
PCI_GNT0#

R406 *1K_NC
R263 *1K_NC

Boot BIOS Strap

		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

USB

23 (5) OC0_1#
23 OC2#

OC0/GPIO59 P4
OC1#/GPIO40 N4
OC2#/GPIO41 N1
OC3#/GPIO42 P5
OC4#/GPIO43 P1
OC5#/GPIO29 P2
OC6#/GPIO30 M3
OC7#/GPIO31 M2
OC8#/GPIO44 P3
OC9#/GPIO45 R1
OC10#/GPIO46 R4
OC11#/GPIO47 R2

USBRBIAS AE5
USBRBIAS# AD5

R376 22.6/F

Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.

ICH9MSFF REV 1.0

RP9 10KX8

OC9# OC5# OC4# OC2# OC3# OC10# OC11#

+3.3V_SUS

R104 10K
R52 10K
R410 10K

PCI Pullups

RP1 8.2KX8

PCI_REQ1# PCI_PLOCK# PCI_STOP# PCI_PERR#
PCI_PIRQD# PCI_DEVSEL# PCI_FRAME# PCI_TRDY#

RP0 8.2KX8

PCI_IRDY# PCI_PIRQC# PCI_PIRQB# PCI_REQ0#
PCI_PIRQA# PCI_SERR# PCI_PIRQH#

+3.3V_RUN

SB_WWAN_PCIE_RST# R361 *8.2K_NC
SB_LOM_PCIE_RST# R133 *8.2K_NC
SB_WPAN_PCIE_RST# R72 *8.2K_NC
SB_WLAN_PCIE_RST# R407 *8.2K_NC
SB_NB_PCIE_RST# R74 *8.2K_NC

SB_WPAN_PCIE_RST# R71 20K
SB_WWAN_PCIE_RST# R364 20K
SB_WLAN_PCIE_RST# R408 20K
SB_LOM_PCIE_RST# R123 20K
SB_NB_PCIE_RST# R73 20K

BIOS should not enable the internal GPIO pull up resistor.

PCI_GNT3# R114 *1K_NC

A16 away override strap.

PCI_GNT#3	Low = A16 swap override enabled. High = Default.

U28B

PCI

AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31

REQ0# G4 PCI_REQ0#
GNT0# E1 PCI_GNT0#
REQ1#/GPIO50 A9 PCI_REQ1#
GNT1#/GPIO51 E12 PCI_GNT1#
REQ2#/GPIO52 B11 SB_WWAN_PCIE_RST#
GNT2#/GPIO53 C10 ICH_GPIO53
REQ3#/GPIO54 D6 SB_LOM_PCIE_RST#
GNT3#/GPIO55 C6 PCI_GNT3#

PAD T94
PAD T67
ICH_GPIO53 11
SB_LOM_PCIE_RST# 29
PAD T24

C/BE0# D10 PCI_C_BE0#
C/BE1# A5 PCI_C_BE1#
C/BE2# E6 PCI_C_BE2#
C/BE3# C9 PCI_C_BE3#

PAD T28
PAD T85
PAD T21
PAD T74

IRDY# C3 PCI_IRDY#
PAR B1 PCI_PAR
PCIRST# T3 PCI_RST# G
DEVSEL# A7 PCI_DEVSEL#
PERR# D4 PCI_PERR#
PLOCK# C5 PCI_PLOCK#
SERR# H5 PCI_SERR#
STOP# A6 PCI_STOP#
TRDY# A2 PCI_TRDY#
FRAME# B8 PCI_FRAME#

PAD T86
PAD T98

PLTRST# A21 PCI_PLTRST#
PCICLK B5 CLK_PCI_ICH
PME# T1 ICH_PME#

CLK_PCI_ICH 15
ICH_PME# 21

Interrupt I/F

PCI_PIRQA# F1 PIRQA#
PCI_PIRQB# F5 PIRQB#
PCI_PIRQC# F2 PIRQC#
PCI_PIRQD# C7 PIRQD#

PIRQE#/GPIO2 G3 SB_WPAN_PCIE_RST#
PIRQF#/GPIO3 G1 SB_WLAN_PCIE_RST#
PIRQG#/GPIO4 F3 SB_NB_PCIE_RST#
PIRQH#/GPIO5 H4 PCI_PIRQH#

SB_WLAN_PCIE_RST# 22
SB_NB_PCIE_RST# 6

ICH9MSFF REV 1.0

+3.3V_SUS

C271 1 2 0.1U/10V

U22 TC7SZ32FU(T5L,F,T)

PLTRST# 6,11,21,22,29

R445 100K

CLK_PCI_ICH

R108 *10_NC
C63 *8.2P_NC

16

Add Buffers as needed for Loading and fanout concerns.

Reserved for EMI.Place resister and cap close to ICH.

QUANTA COMPUTER

Title	ICH9-M(USB,PCIE,DMI)		
Size	Document Number SS5		Rev 1A
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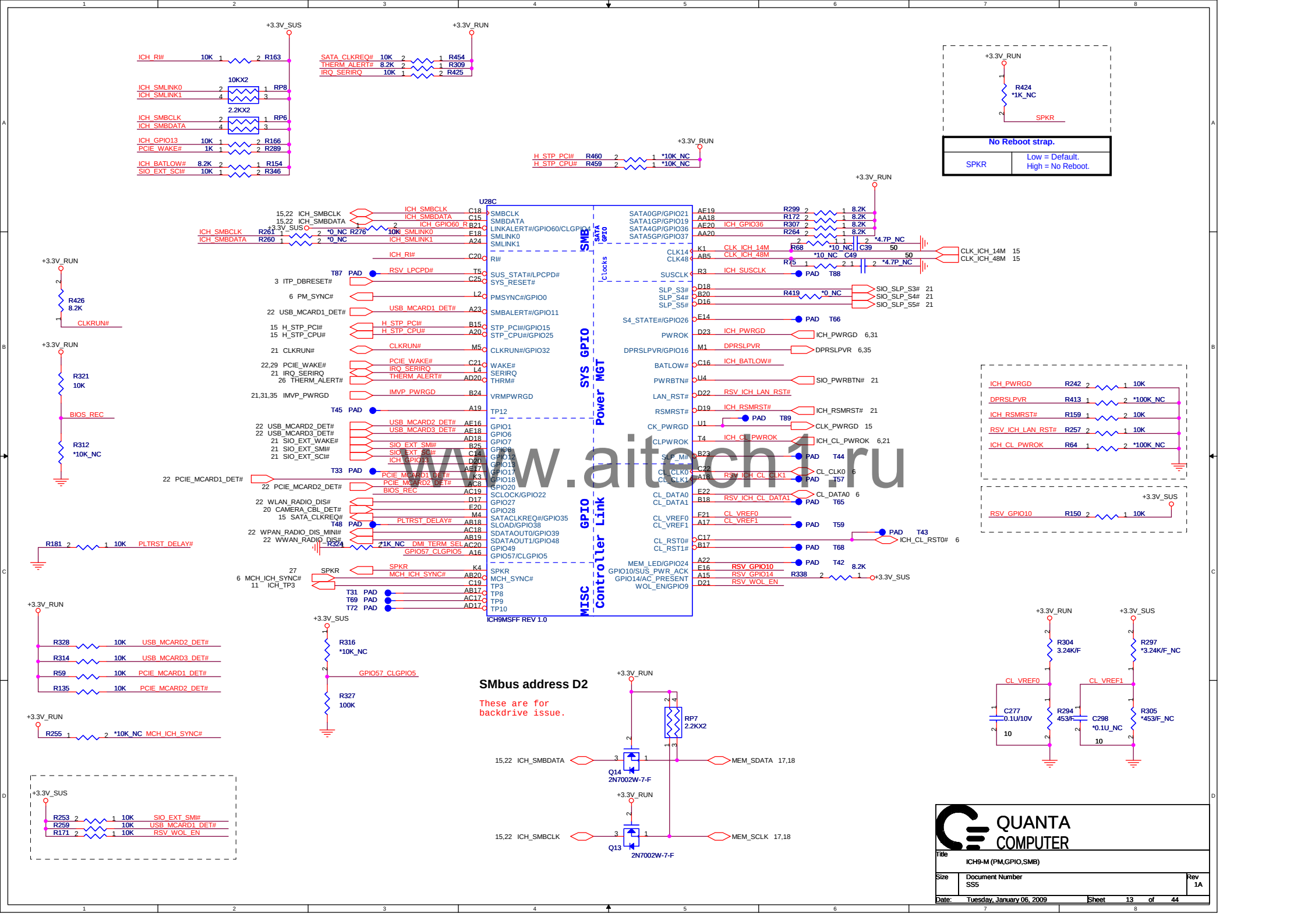
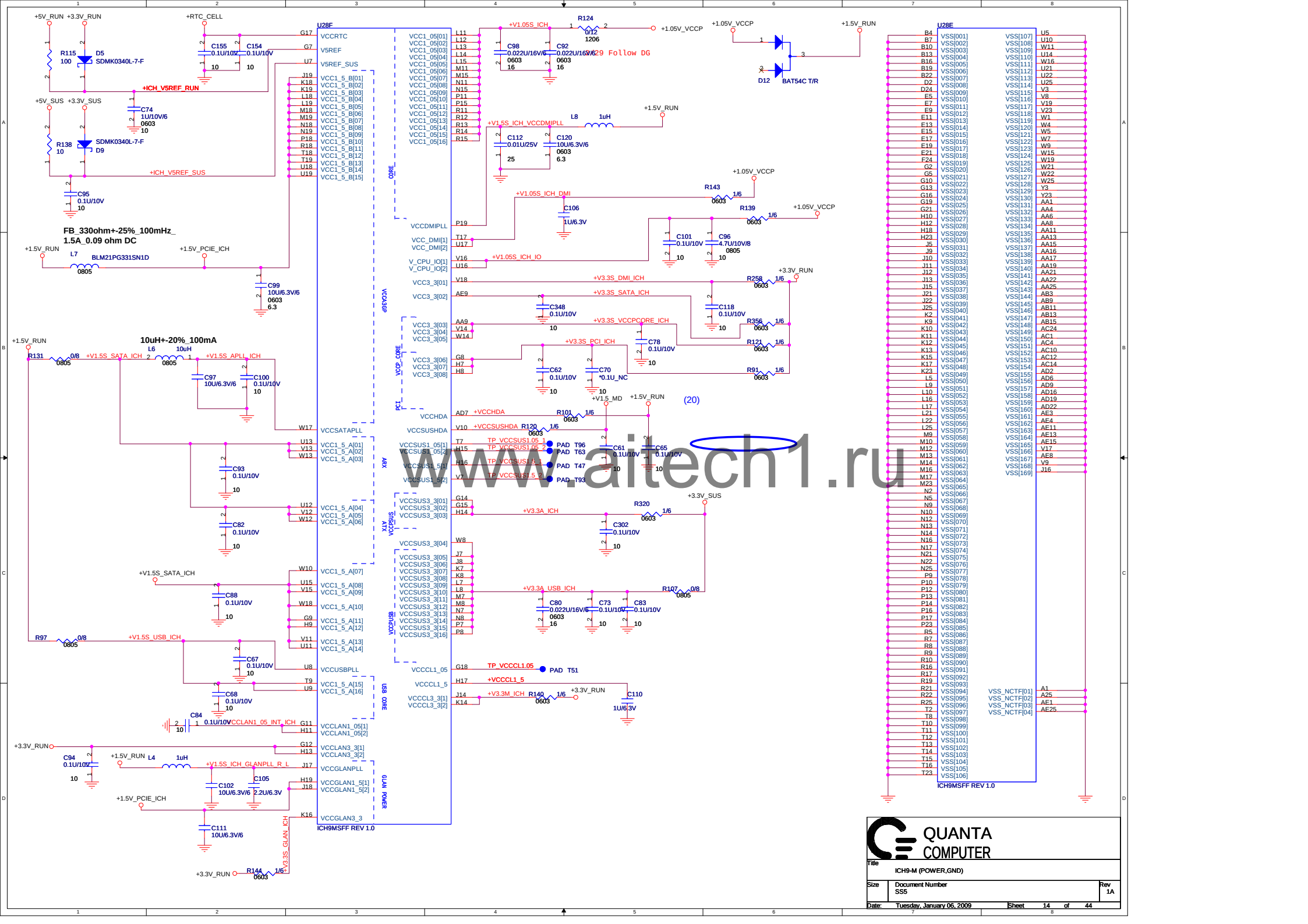
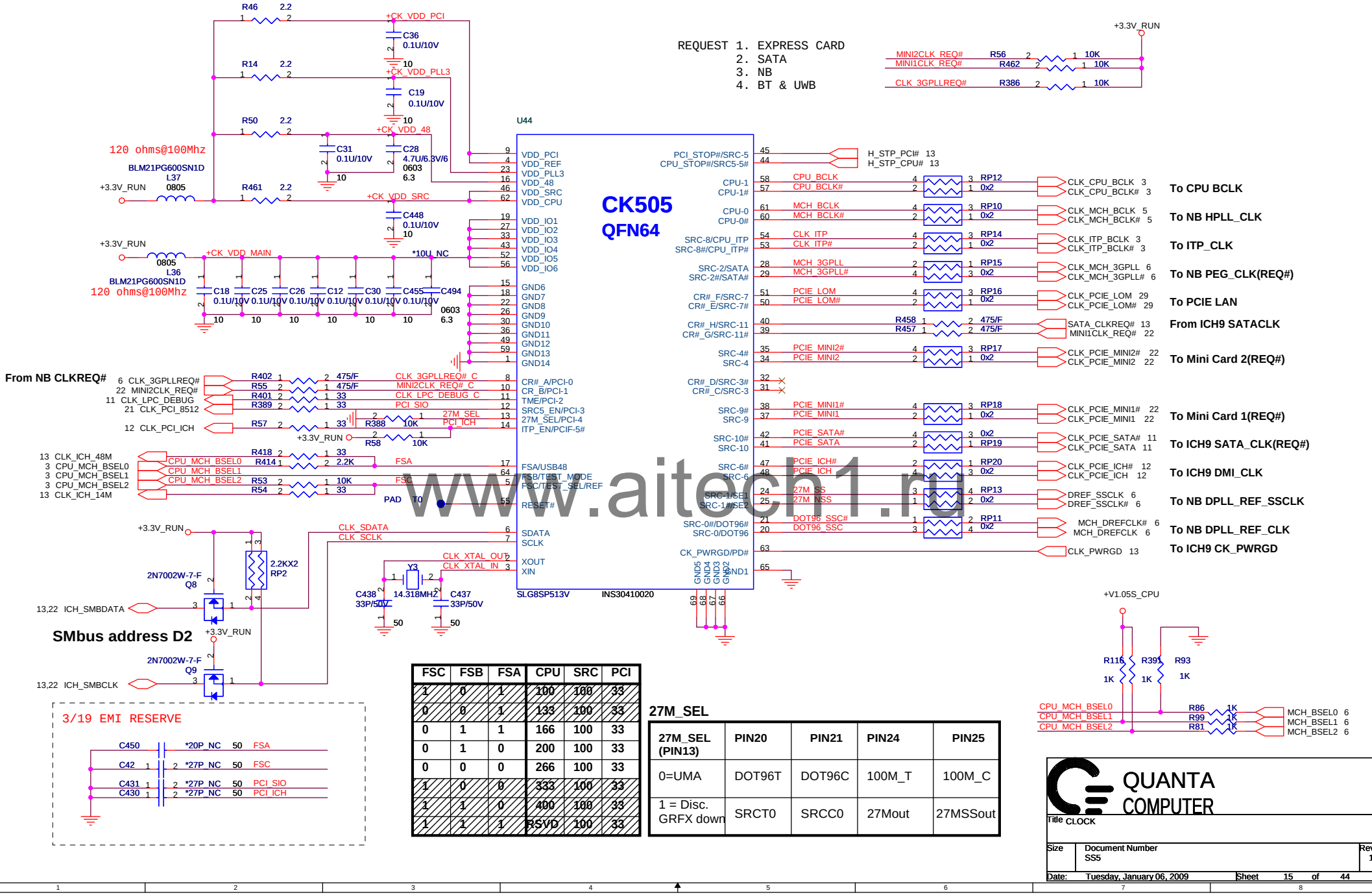

U28C
ICH9MSFF REV 1.0
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SMBus address D2
These are for backdrive issue.
No Reboot strap.
SPKR
Low = Default.
High = No Reboot.
www.aitech1.ru
QUANTA COMPUTER
Title
ICH9-M (PM,GPIO,SMB)
Size
Document Number
SS5
Rev
1A
Date:
Tuesday, January 06, 2009
Sheet
13
of
44





FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

27M_SEL

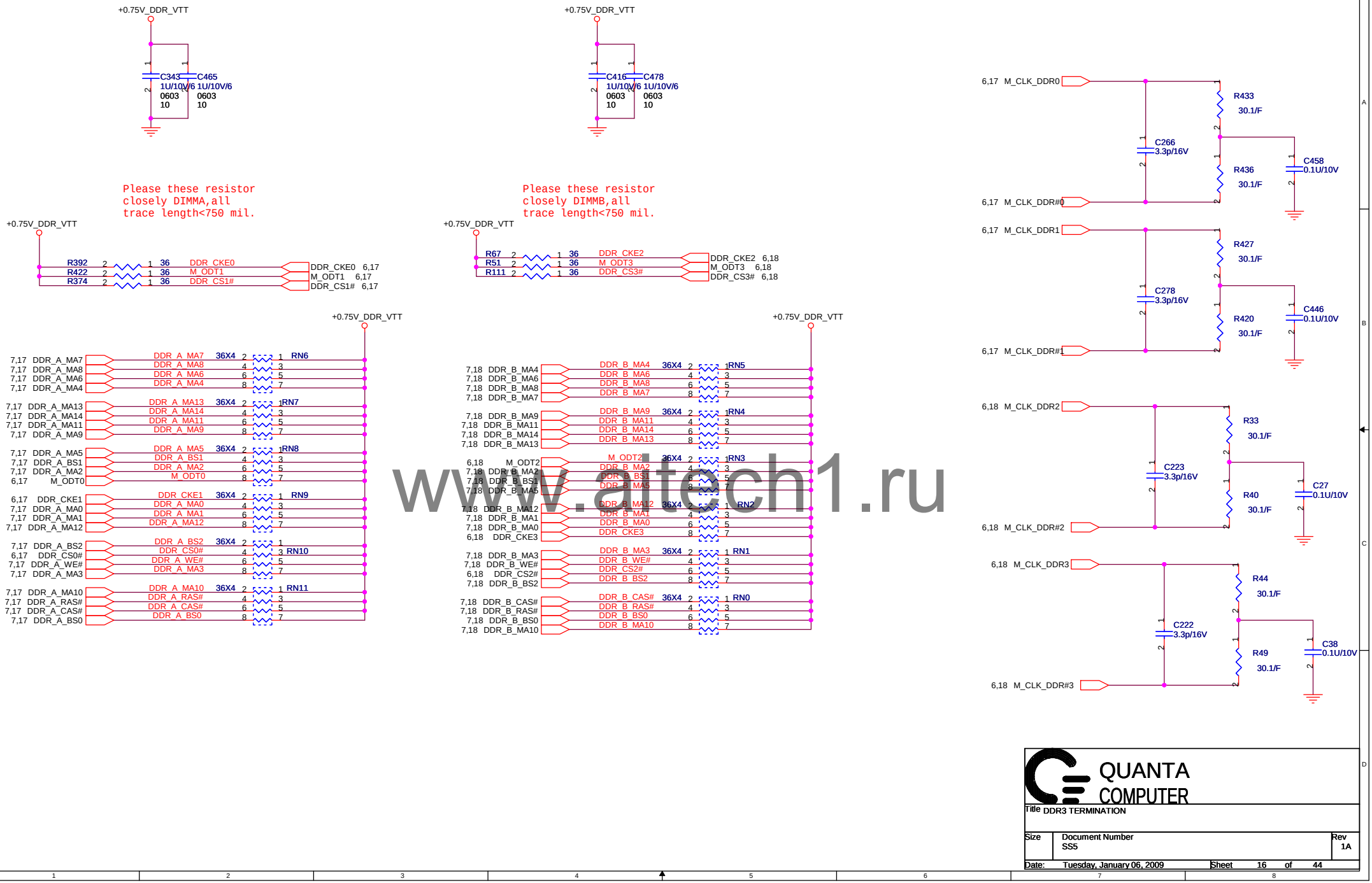
27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	100M_T	100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout

QUANTA COMPUTER

Title CLOCK

Size | Document Number SS5 | Rev 1A

Date: Tuesday, January 06, 2009 | Sheet 15 of 44


+0.75V_DDR_VTT
C343 1U/10V/6 0603 10
C465 1U/10V/6 0603 10
+0.75V_DDR_VTT
C416 1U/10V/6 0603 10
C478 1U/10V/6 0603 10
Please these resistor closely DIMMA,all trace length<750 mil.
Please these resistor closely DIMMB,all trace length<750 mil.
+0.75V_DDR_VTT
R392 R422 R374
DDR_CKE0 M_ODT1 DDR_CS1#
DDR_CKE0 6,17
M_ODT1 6,17
DDR_CS1# 6,17
+0.75V_DDR_VTT
R67 R51 R111
DDR_CKE2 M_ODT3 DDR_CS3#
DDR_CKE2 6,18
M_ODT3 6,18
DDR_CS3# 6,18
+0.75V_DDR_VTT
7,17 DDR_A_MA7
7,17 DDR_A_MA8
7,17 DDR_A_MA6
7,17 DDR_A_MA4
DDR_A_MA7 DDR_A_MA8 DDR_A_MA6 DDR_A_MA4
36X4 RN6
7,17 DDR_A_MA13
7,17 DDR_A_MA14
7,17 DDR_A_MA11
7,17 DDR_A_MA9
DDR_A_MA13 DDR_A_MA14 DDR_A_MA11 DDR_A_MA9
36X4 RN7
7,17 DDR_A_MA5
7,17 DDR_A_BS1
7,17 DDR_A_MA2
6,17 M_ODT0
DDR_A_MA5 DDR_A_BS1 DDR_A_MA2 M_ODT0
36X4 RN8
6,17 DDR_CKE1
7,17 DDR_A_MA0
7,17 DDR_A_MA1
7,17 DDR_A_MA12
DDR_CKE1 DDR_A_MA0 DDR_A_MA1 DDR_A_MA12
36X4 RN9
7,17 DDR_A_BS2
6,17 DDR_CS0#
7,17 DDR_A_WE#
7,17 DDR_A_MA3
DDR_A_BS2 DDR_CS0# DDR_A_WE# DDR_A_MA3
36X4 RN10
7,17 DDR_A_MA10
7,17 DDR_A_RAS#
7,17 DDR_A_CAS#
7,17 DDR_A_BS0
DDR_A_MA10 DDR_A_RAS# DDR_A_CAS# DDR_A_BS0
36X4 RN11
+0.75V_DDR_VTT
7,18 DDR_B_MA4
7,18 DDR_B_MA6
7,18 DDR_B_MA8
7,18 DDR_B_MA7
DDR_B_MA4 DDR_B_MA6 DDR_B_MA8 DDR_B_MA7
36X4 RN5
7,18 DDR_B_MA9
7,18 DDR_B_MA11
7,18 DDR_B_MA14
7,18 DDR_B_MA13
DDR_B_MA9 DDR_B_MA11 DDR_B_MA14 DDR_B_MA13
36X4 RN4
6,18 M_ODT2
7,18 DDR_B_MA2
7,18 DDR_B_BS1
7,18 DDR_B_MA5
M_ODT2 DDR_B_MA2 DDR_B_BS1 DDR_B_MA5
36X4 RN3
7,18 DDR_B_MA12
7,18 DDR_B_MA1
7,18 DDR_B_MA0
6,18 DDR_CKE3
DDR_B_MA12 DDR_B_MA1 DDR_B_MA0 DDR_CKE3
36X4 RN2
7,18 DDR_B_MA3
7,18 DDR_B_WE#
6,18 DDR_CS2#
7,18 DDR_B_BS2
DDR_B_MA3 DDR_B_WE# DDR_CS2# DDR_B_BS2
36X4 RN1
7,18 DDR_B_CAS#
7,18 DDR_B_RAS#
7,18 DDR_B_BS0
7,18 DDR_B_MA10
DDR_B_CAS# DDR_B_RAS# DDR_B_BS0 DDR_B_MA10
36X4 RN0
6,17 M_CLK_DDR0
R433 30.1/F
C266 3.3p/16V
R436 30.1/F
C458 0.1U/10V
6,17 M_CLK_DDR#0
6,17 M_CLK_DDR1
R427 30.1/F
C278 3.3p/16V
R420 30.1/F
C446 0.1U/10V
6,17 M_CLK_DDR#1
6,18 M_CLK_DDR2
R33 30.1/F
C223 3.3p/16V
R40 30.1/F
C27 0.1U/10V
6,18 M_CLK_DDR#2
6,18 M_CLK_DDR3
R44 30.1/F
C222 3.3p/16V
R49 30.1/F
C38 0.1U/10V
6,18 M_CLK_DDR#3
QUANTA COMPUTER
Title DDR3 TERMINATION
Size
Document Number SS5
Rev 1A
Date: Tuesday, January 06, 2009
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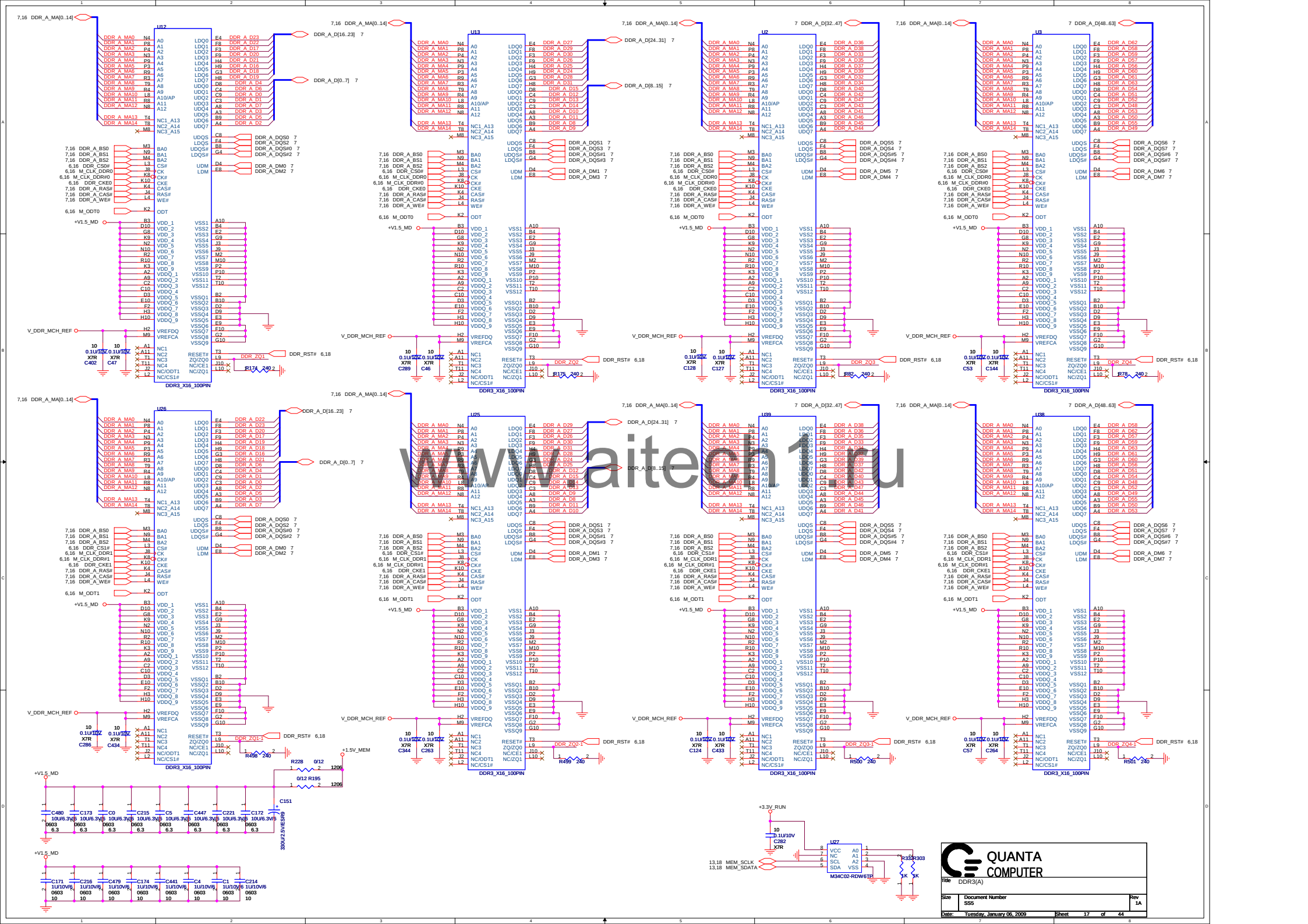
U12
U13
U2
U3
U26
U25
U39
U38
DDR3_X16_100PIN
M34C02-RDW6TP
QUANTA COMPUTER
Title DDR3(A)
Size Document Number SS5 Rev 1A
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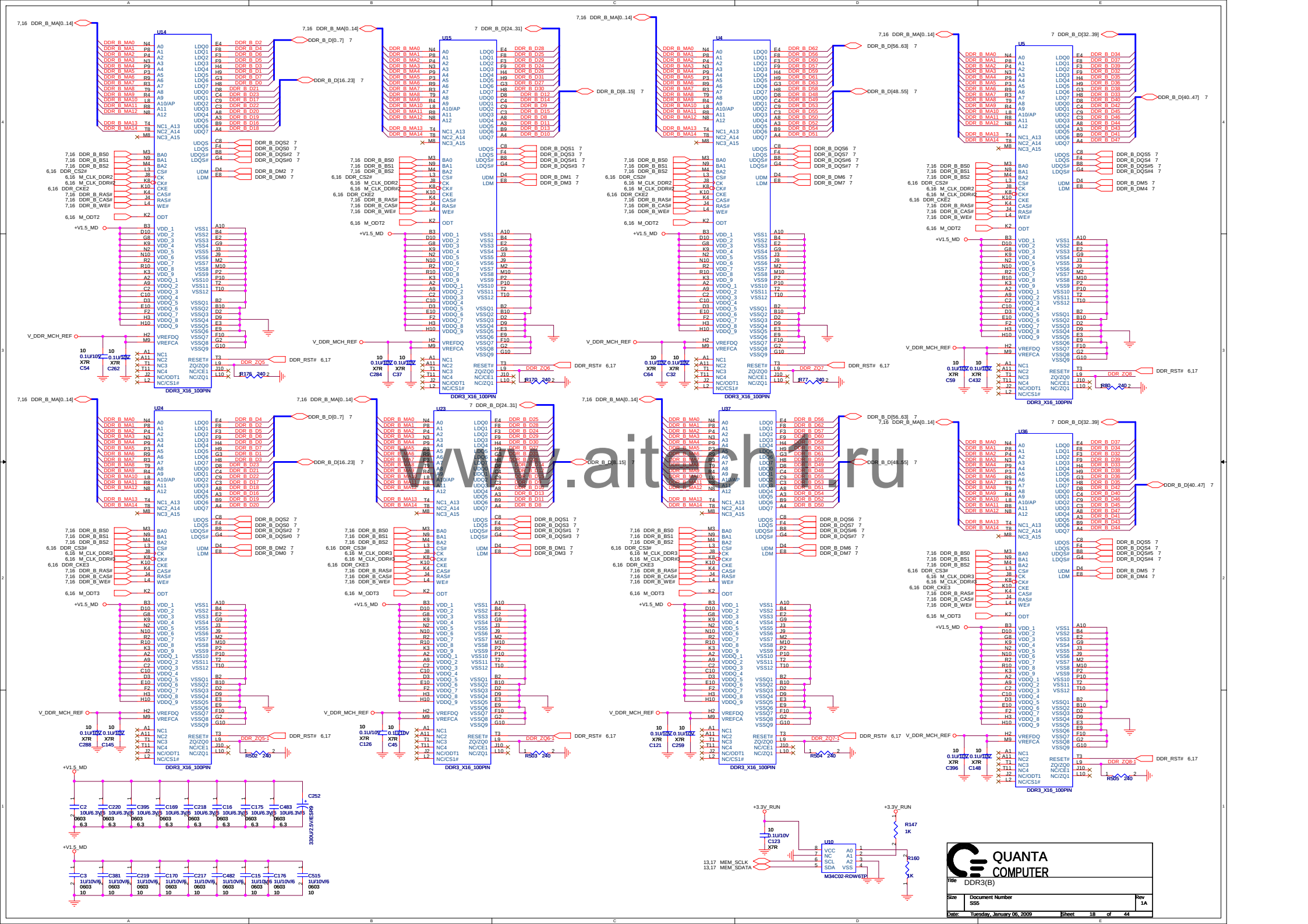

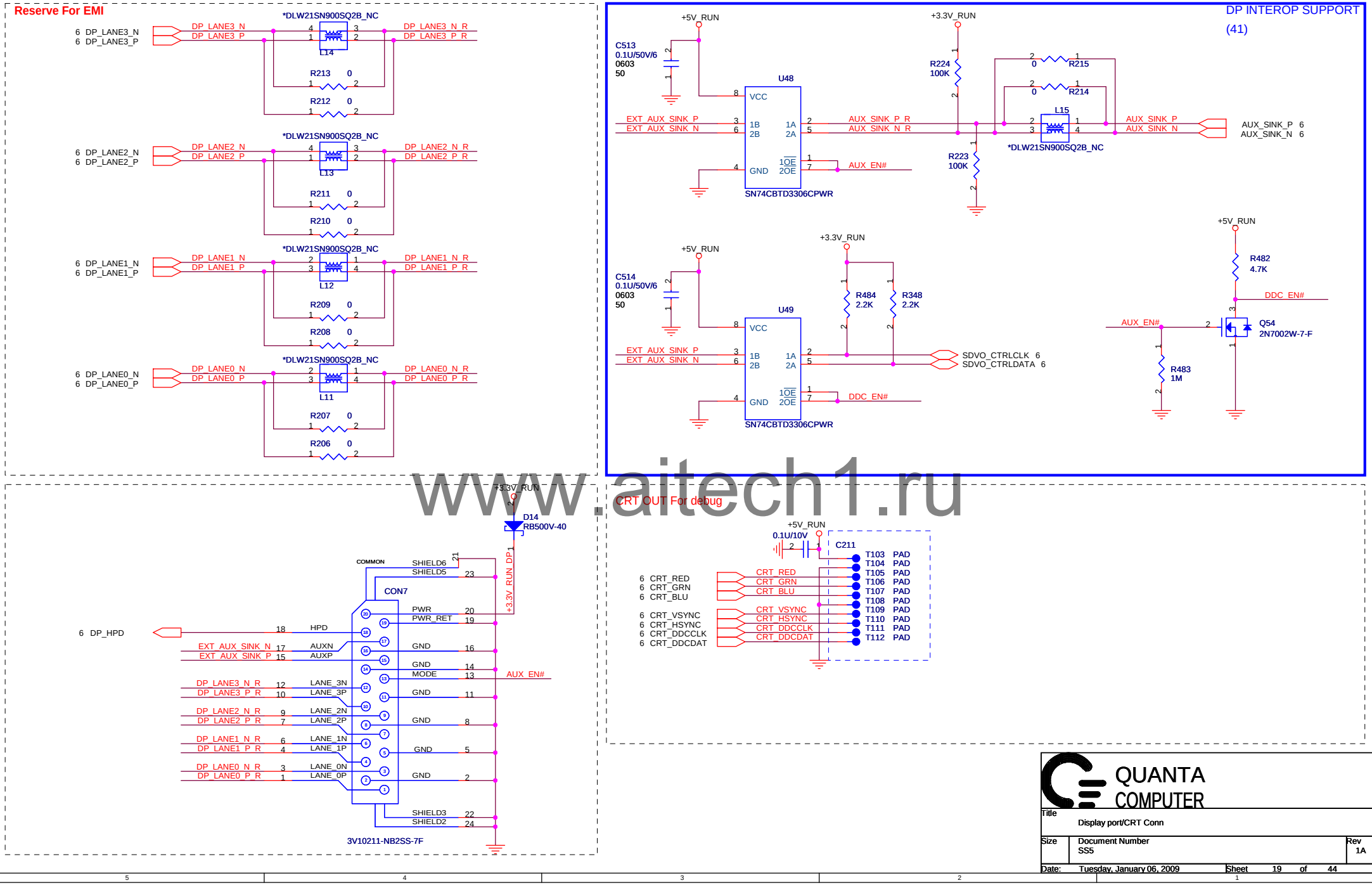

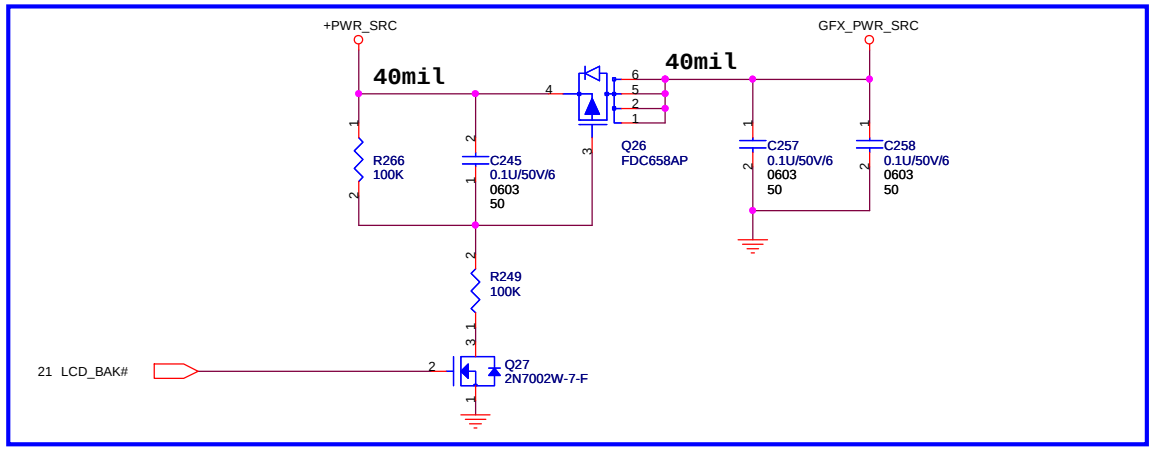

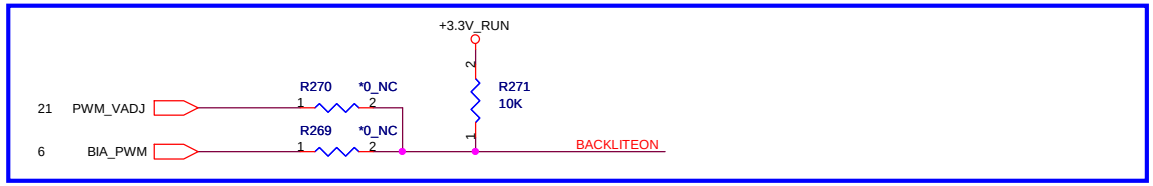

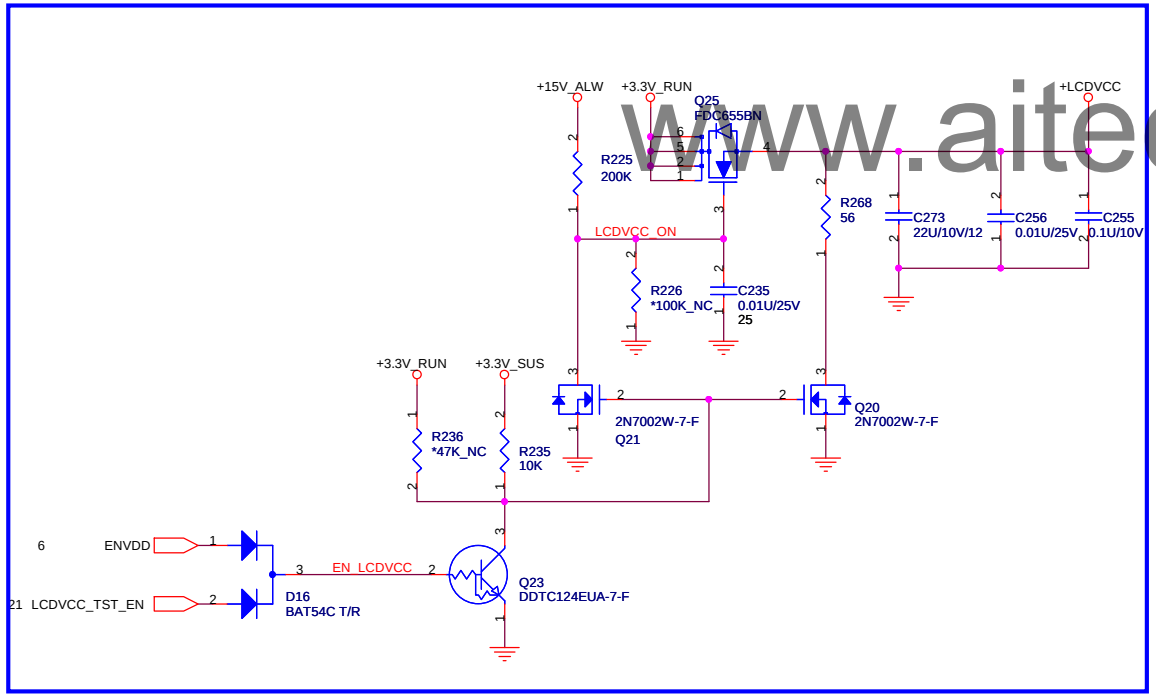

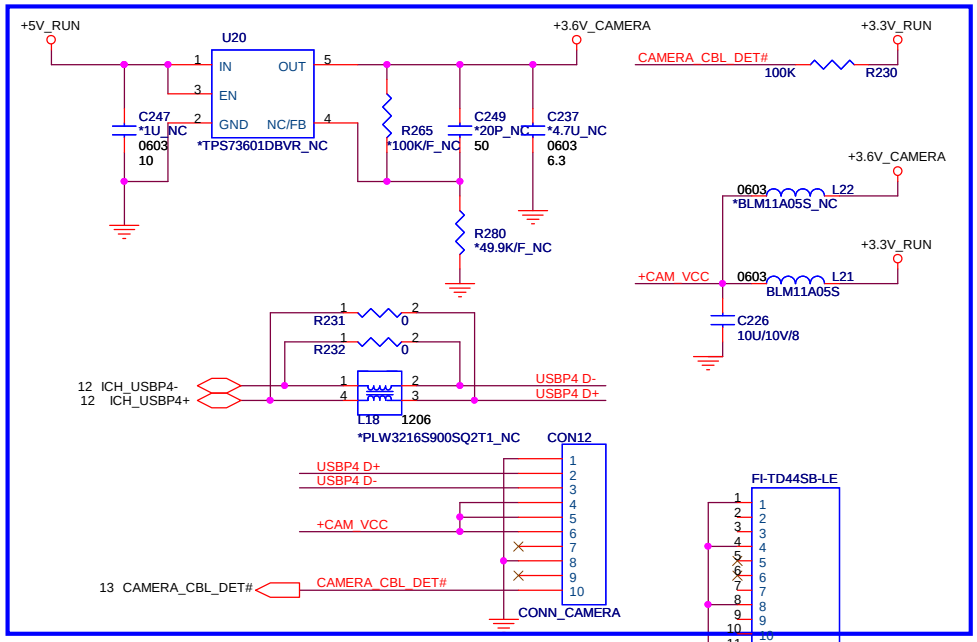

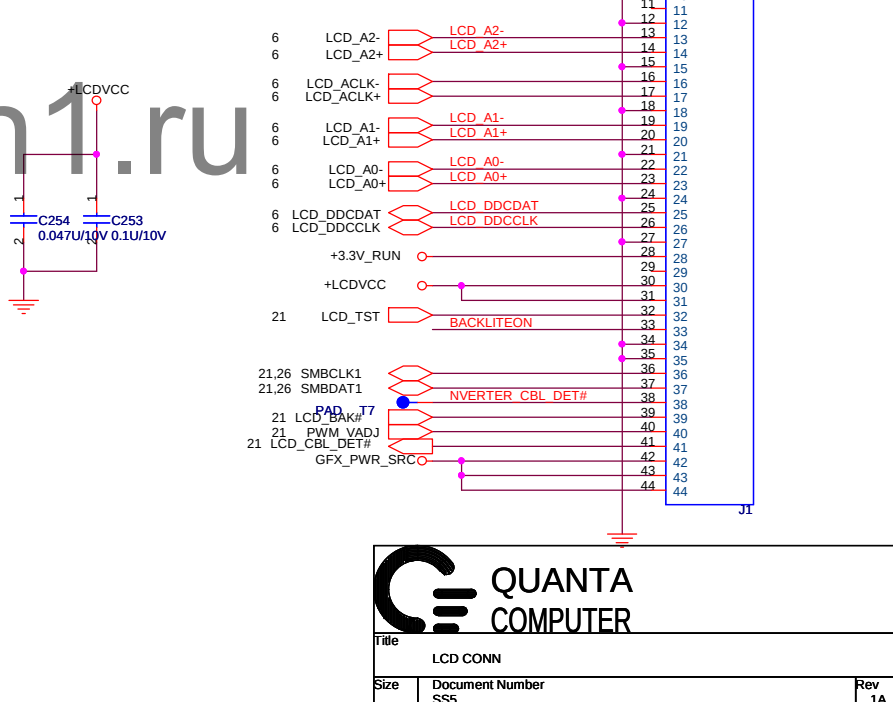

QUANTA COMPUTER

Title	LCD CONN	
Size	Document Number SS5	Rev 1A
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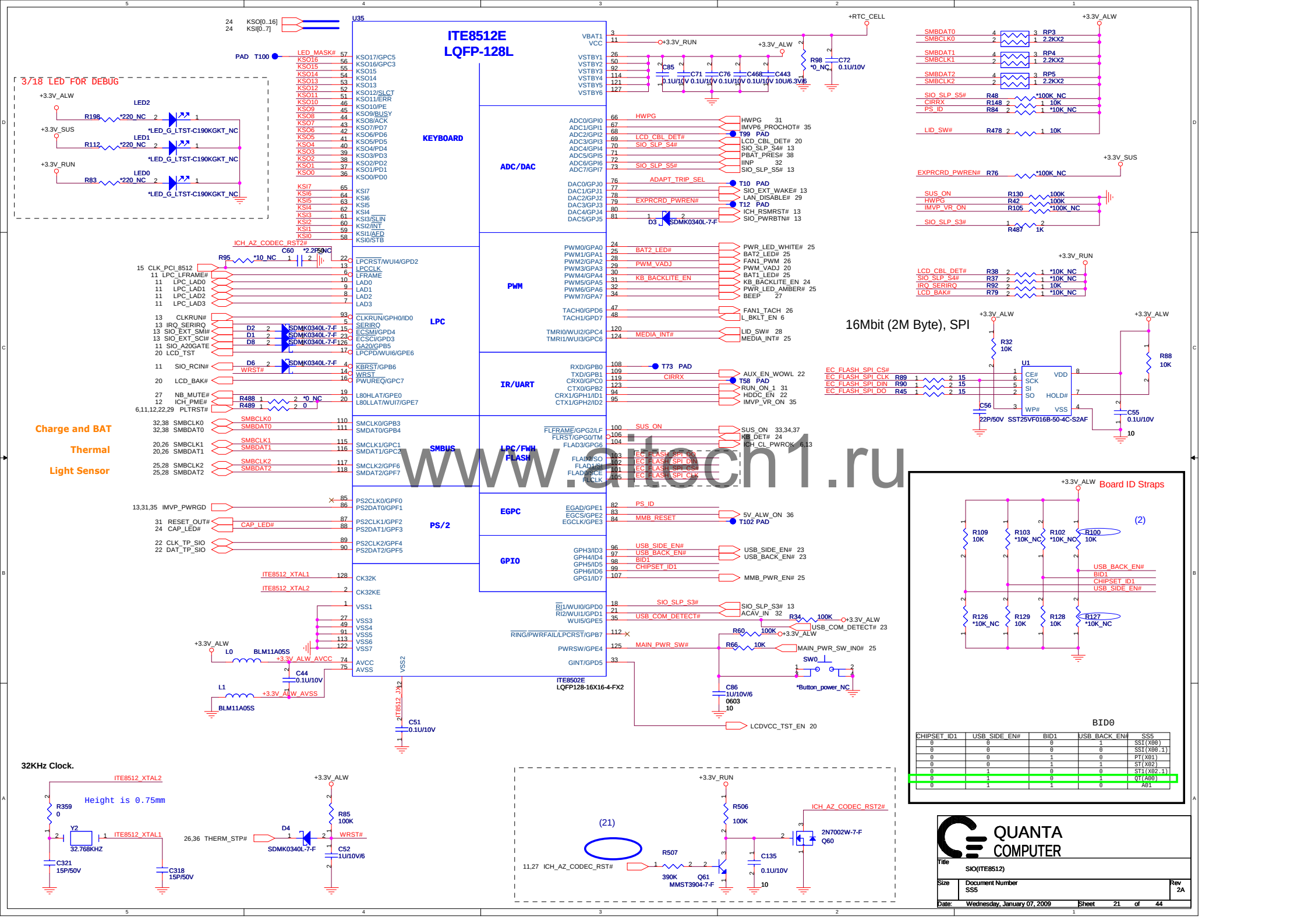

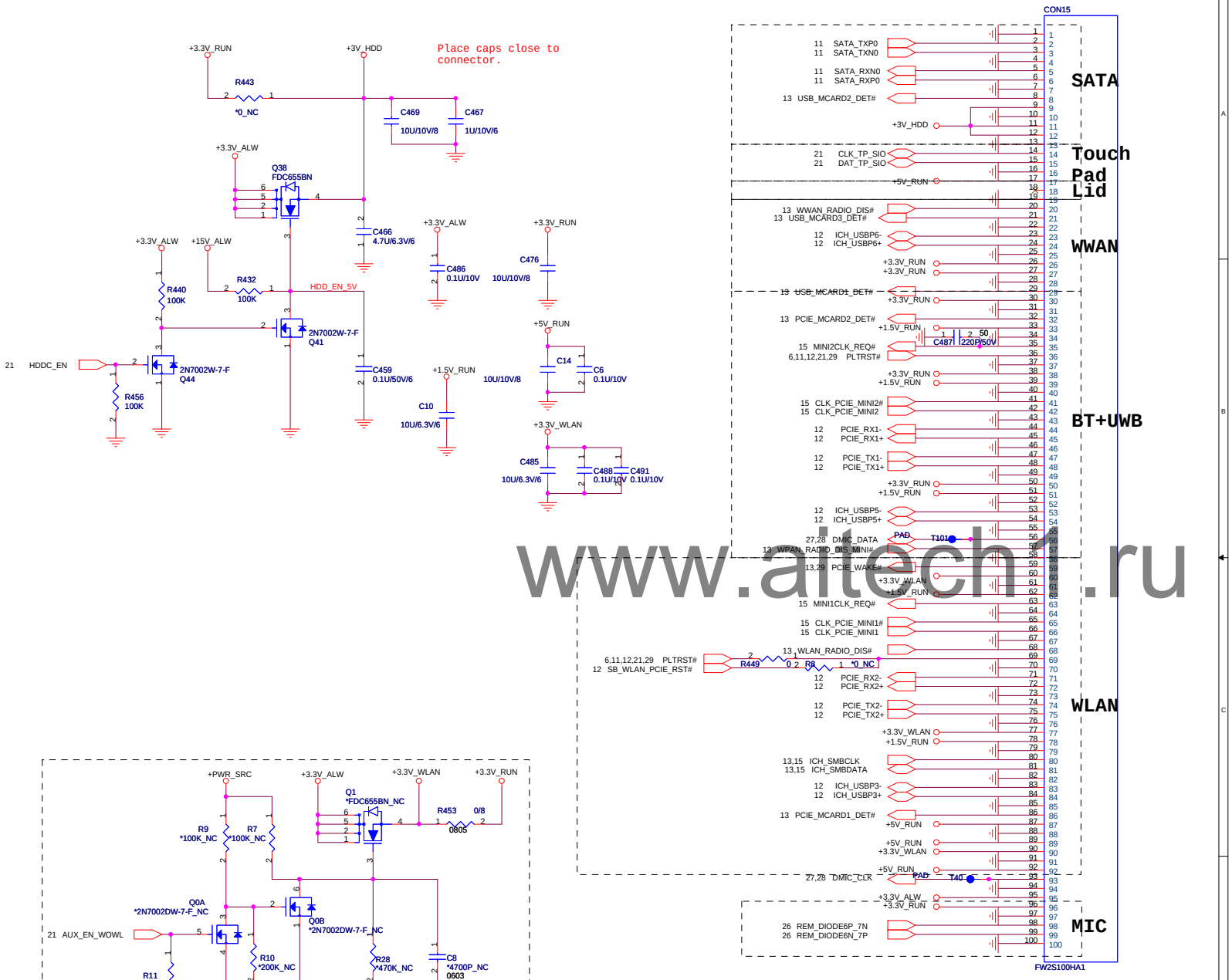

QUANTA COMPUTER

Title	All in one_100PIN	
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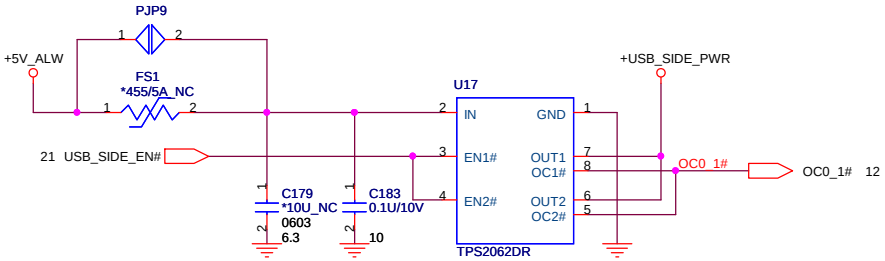
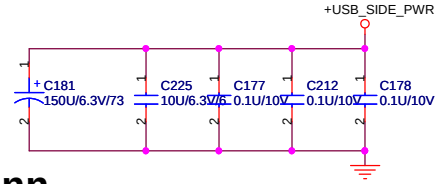
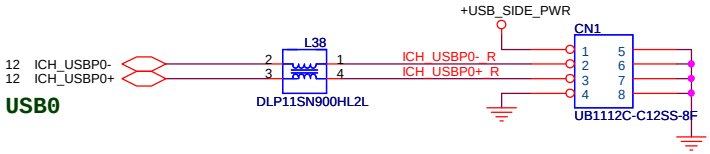
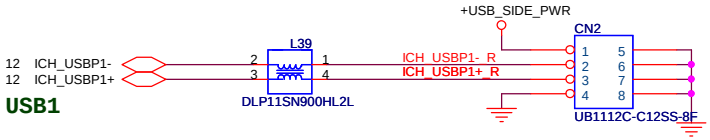
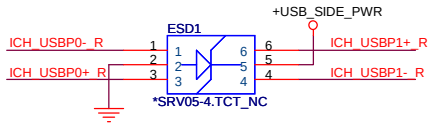
USB x2 Conn



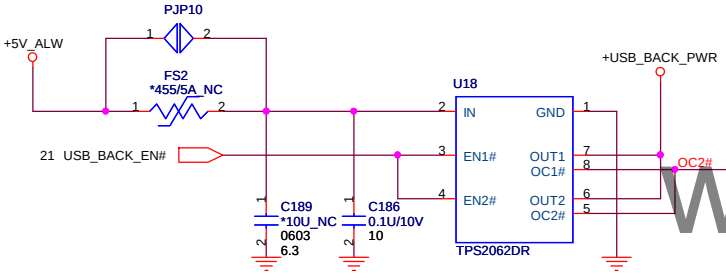


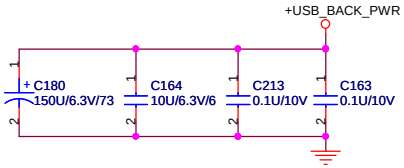




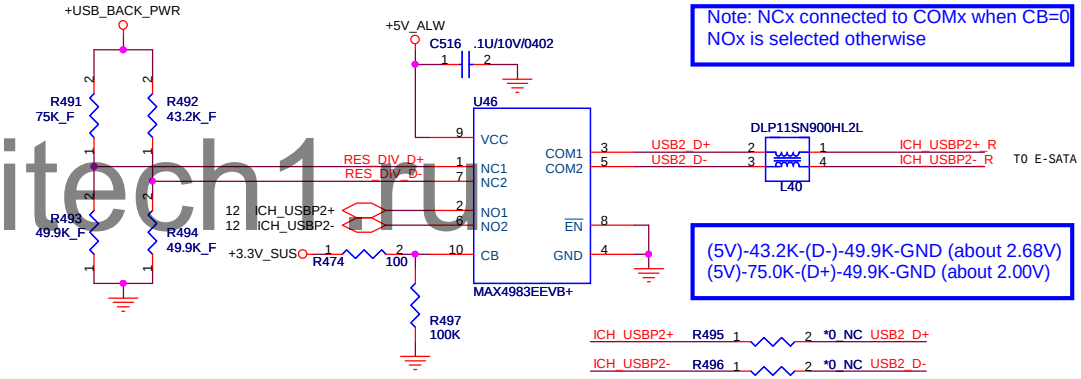


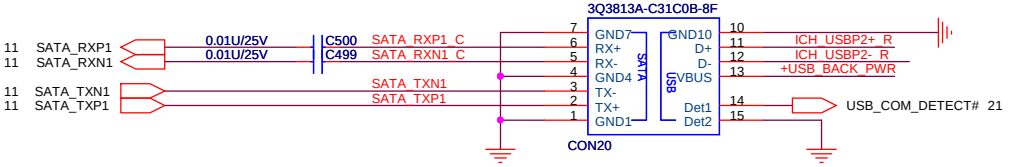
SATA + USB Conn





BATTERY STATUS LED 1





QUANTA COMPUTER

Title	SERIAL PORT & USB	
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KEYBOARD CONNECTOR

CP0 *100PX4_NC: 8 KSI6, 7 KSI4, 6 KSI2, 5 KSI5 — 1206 50
CP1 *100PX4_NC: 8 KSO5, 7 KSI0, 6 KSI3, 5 KSI1 — 1206 50
CP2 *100PX4_NC: 8 KSO4, 7 KSO7, 6 KSO6, 5 KSO8 — 1206 50
CP3 *100PX4_NC: 8 KSO3, 7 KSO1, 6 KSO2, 5 KSO0 — 1206 50
CP4 *100PX4_NC: 8 KSO12, 7 KSO16, 6 KSO15, 5 KSO13 — 1206 50
CP5 *100PX4_NC: 8 KSO14, 7 KSO9, 6 KSO11, 5 KSO10 — 1206 50

C495 *100P_NC — KSI7

CAP_LED#

+3.3V_RUN, +3.3V_RUN, +5V_RUN, +5V_RUN
R452 100K, R450 100K
21 CAP_LED#
Q56 2N7002W-7-F
Q59 DDTA114YUA-7-F (47K, 10K)
R446 220 CAP_LED_L

KB LED CONN

21 KB_BACKLITE_EN — R110 *0_NC — KB_BACKLITE
+5V_RUN
CON16 1 2 3 4 — FH33-4S-1SH(10)
KB_BACKLITE
Q39 SI2304BDS-T1-E3
21 KB_BACKLITE_EN

+3.3V_ALW — R465 1 2 10K
21 KB_DET#
21 KSO[0..16]
21 KSI[0..7]

CON19 — FH31H-64(32)SB-1SH(05)
32 KSI7, 31 KSI6, 30 KSI4, 29 KSI2, 28 KSI5, 27 KSI1, 26 KSI3, 25 KSI0, 24 KSO5, 23 KSO4, 22 KSO7, 21 KSO6, 20 KSO8, 19 KSO3, 18 KSO1, 17 KSO2, 16 KSO0, 15 KSO12, 14 KSO16, 13 KSO15, 12 KSO13, 11 KSO14, 10 KSO9, 9 KSO11, 8 KSO10
7 6 5 4 3 2 1 — CAP_LED_L
33 34

100P CAPS CLOSE TO JKB1

QUANTA COMPUTER

Title	TOUCH PAD, BULE TOOTH & FIR	
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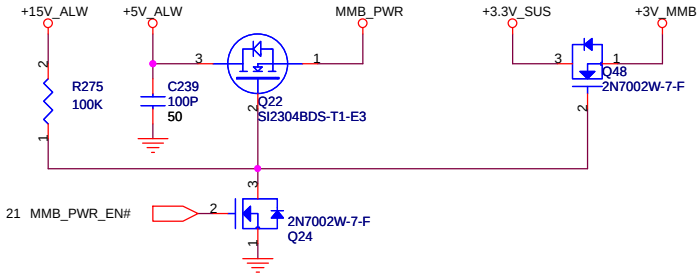
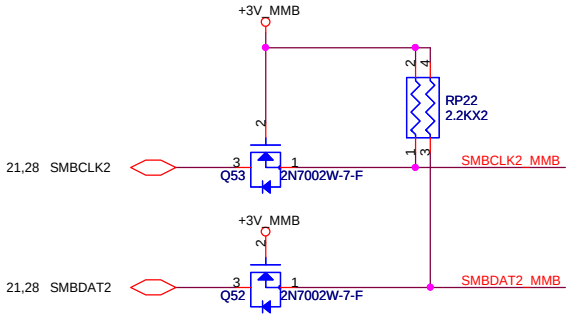
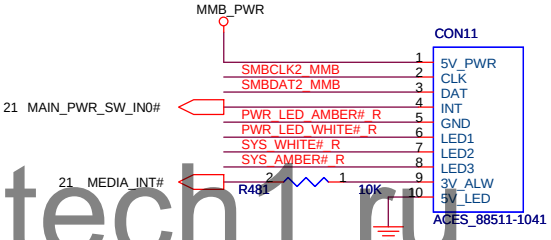
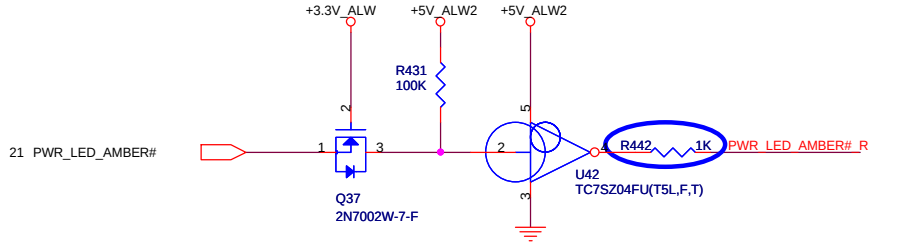




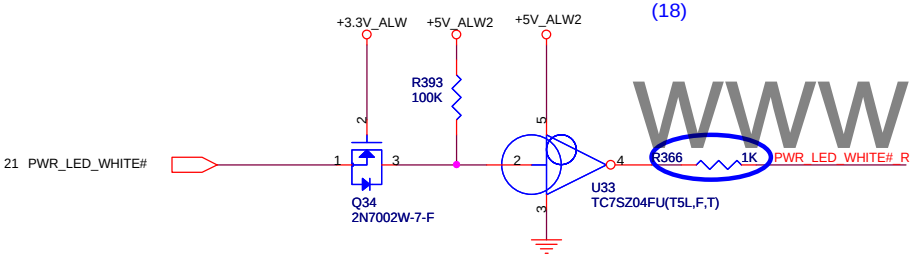


POWER LED

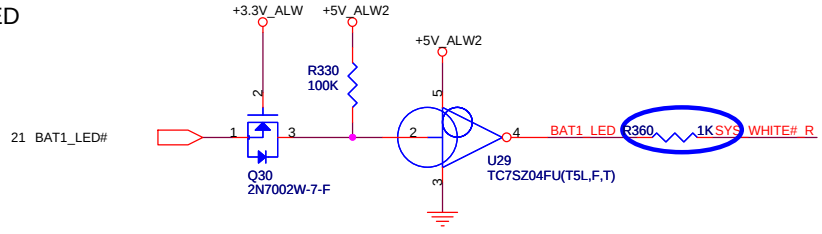
Function board CONN



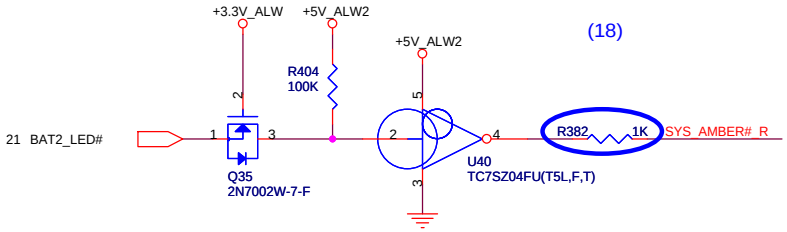
(18)



System LED



(18)



System Power State	Power Source	Battery Charge State	LED Behavior
On (S0)	AC	0-100%	Off
On (S0)	DC	< 10%	Flash Amber
On (S0)	DC	> 10%	Off
Standby (S3)	AC	0-100%	"Breathe" White
Standby (S3)	DC	< 10%	Flash Amber
Standby (S3)	DC	> 10%	"Breathe" White
Off or Hibernate (S4/S5)	AC	< 90%	Solid Amber
Off or Hibernate (S4/S5)	AC	> 90%	Solid White
Off or Hibernate (S4/S5)	DC	0-100%	Off

QUANTA COMPUTER

Title: SWITCH, KEYBOARD & LED

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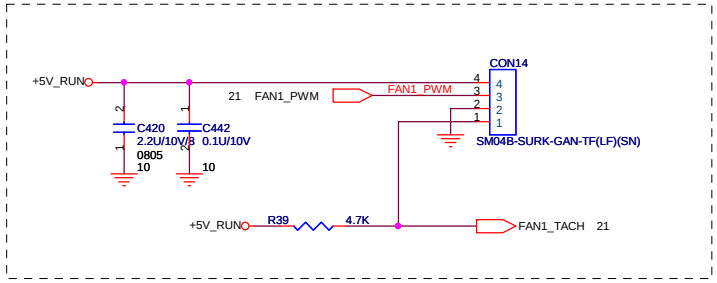


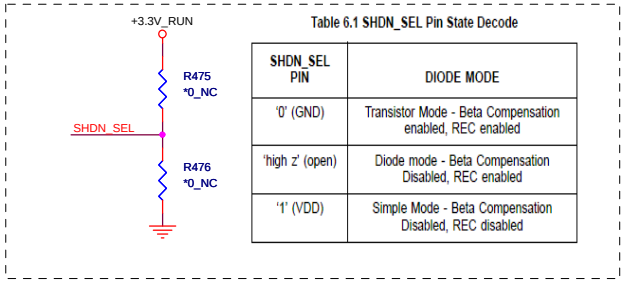
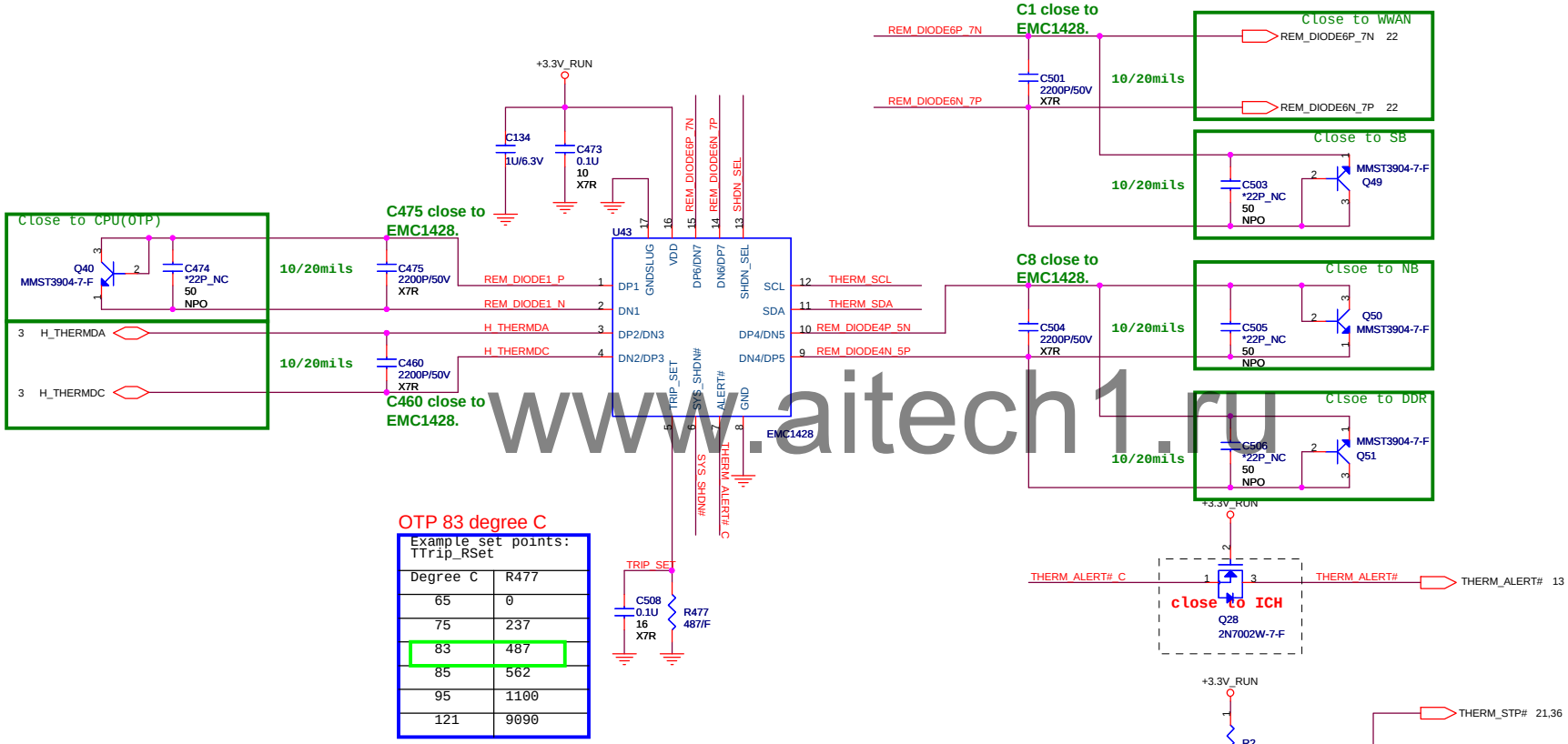


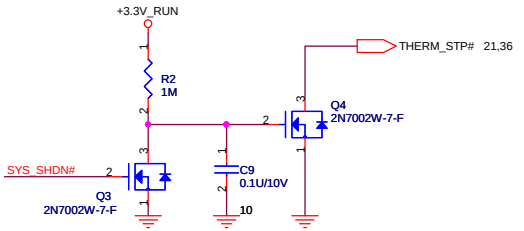
Table 6.1 SHDN_SEL Pin State Decode

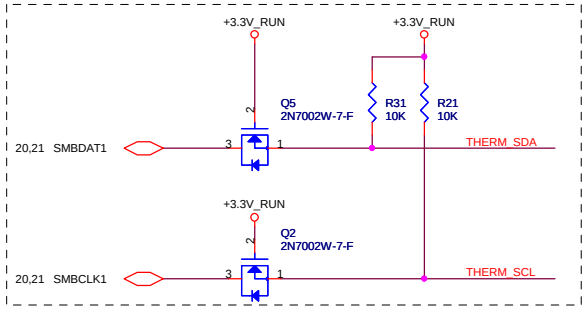
SHDN_SEL PIN	DIODE MODE
'0' (GND)	Transistor Mode - Beta Compensation enabled, REC enabled
'high z' (open)	Diode mode - Beta Compensation Disabled, REC enabled
'1' (VDD)	Simple Mode - Beta Compensation Disabled, REC disabled

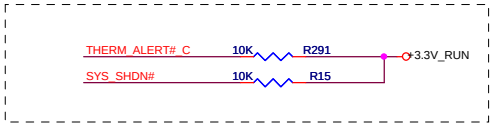


OTP 83 degree C

Example set points: TTrip_RSet	
Degree C	R477
65	0
75	237
83	487
85	562
95	1100
121	9090







QUANTA COMPUTER

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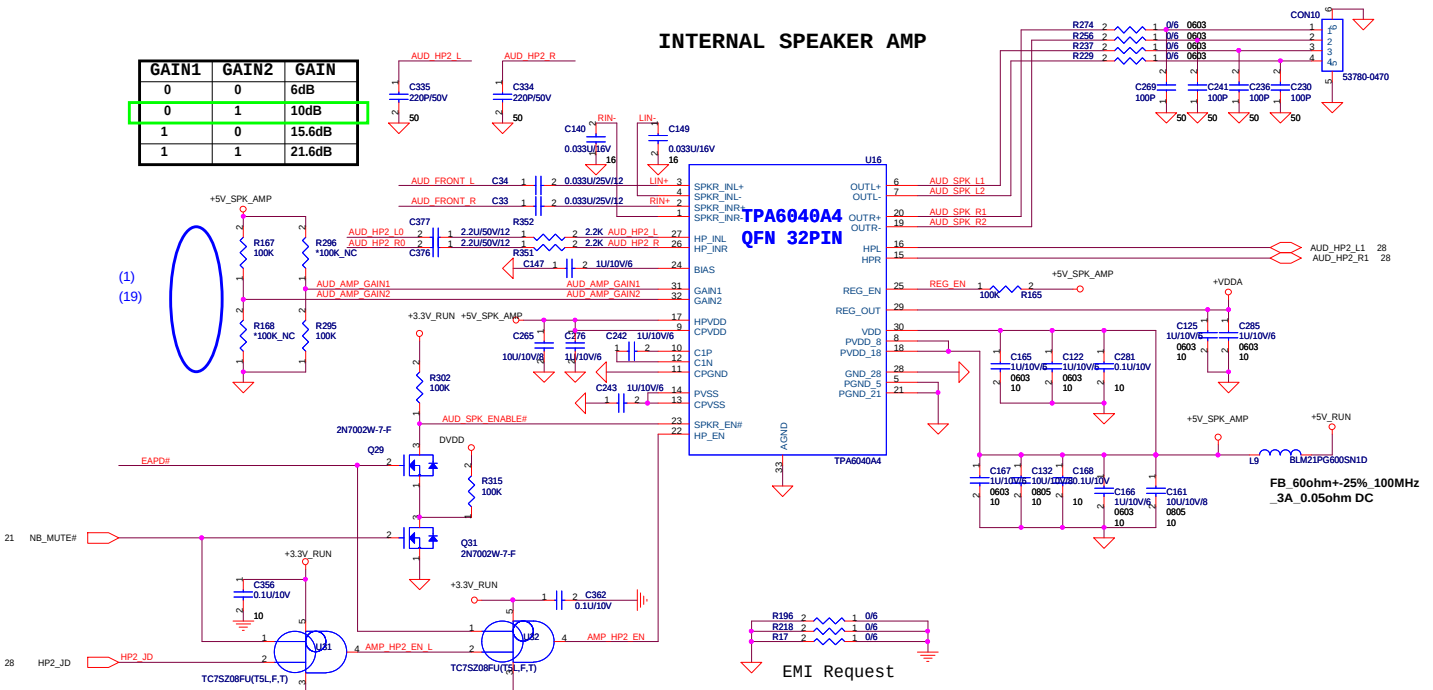
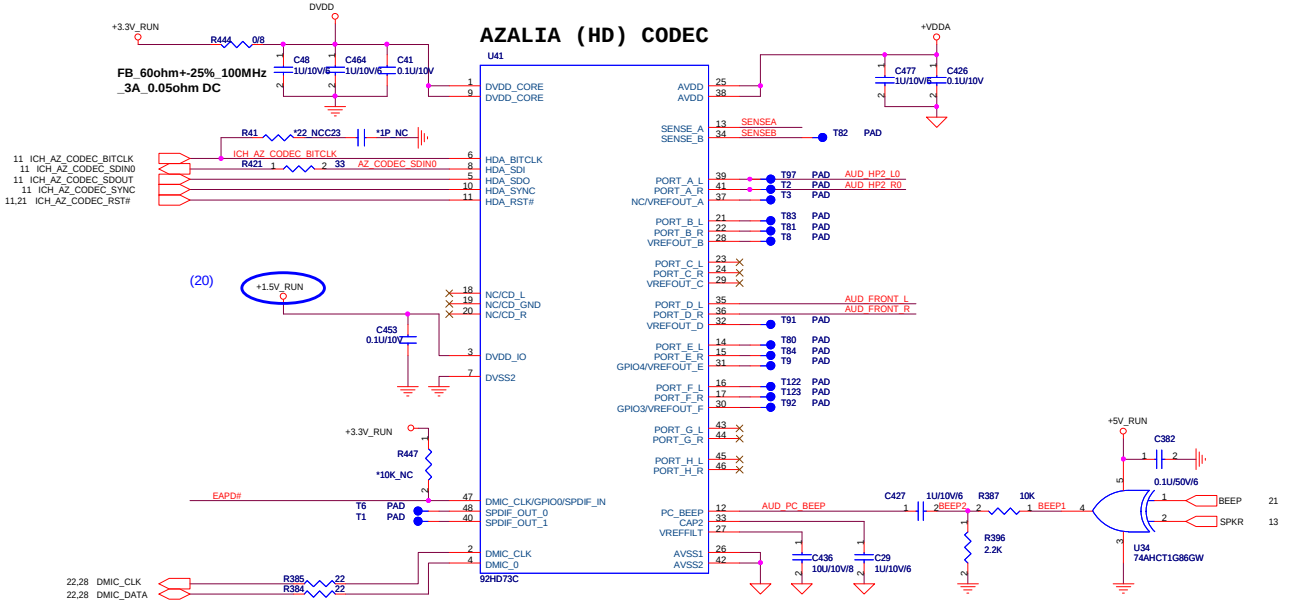
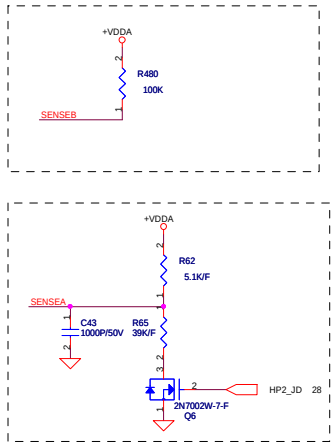
INTERNAL SPEAKER AMP

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



AZALIA (HD) CODEC





Title	Azelia CODEC
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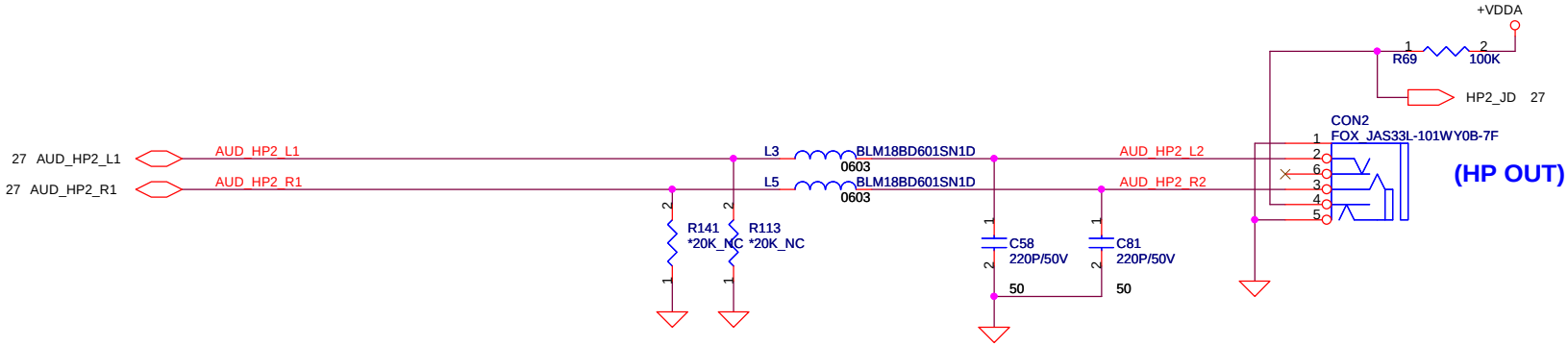

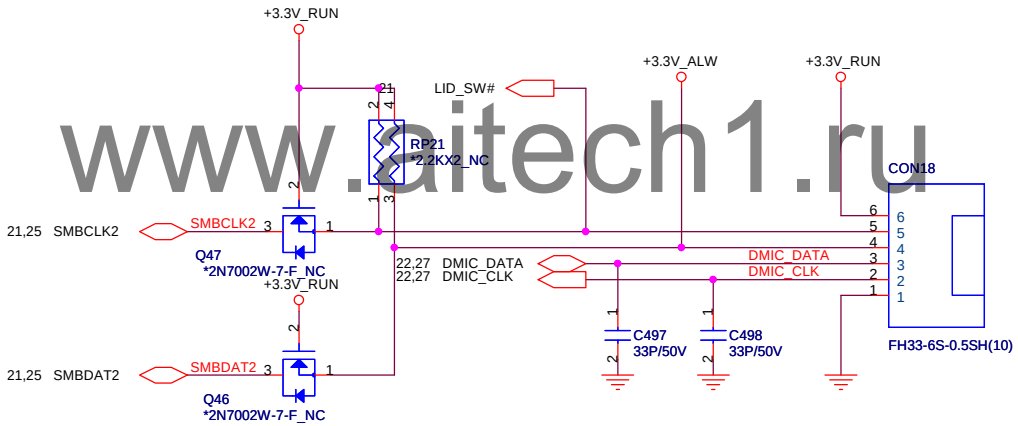

QUANTA COMPUTER

Title	AUDIO CONN	
Size	Document Number SS5	Rev 1A
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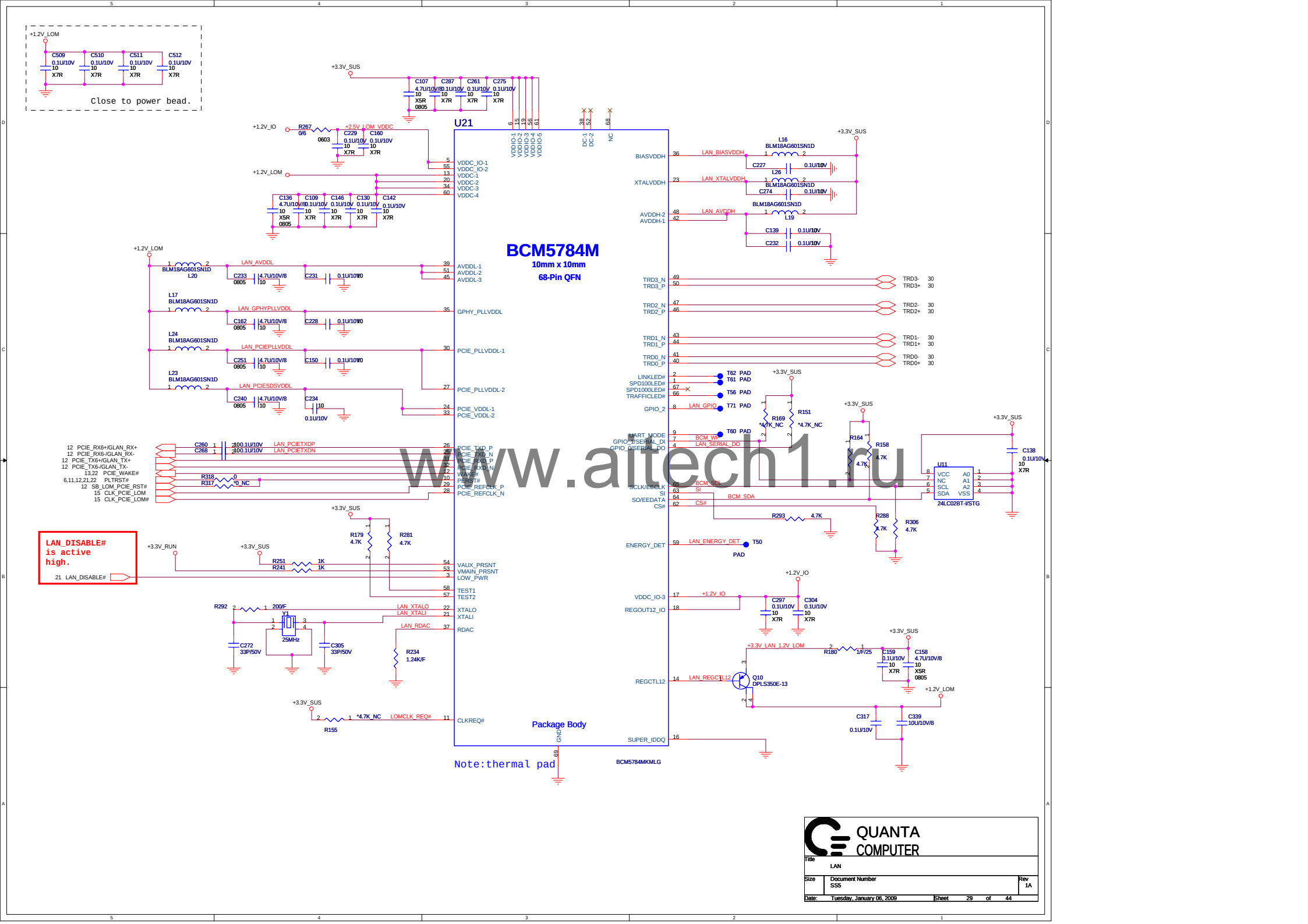

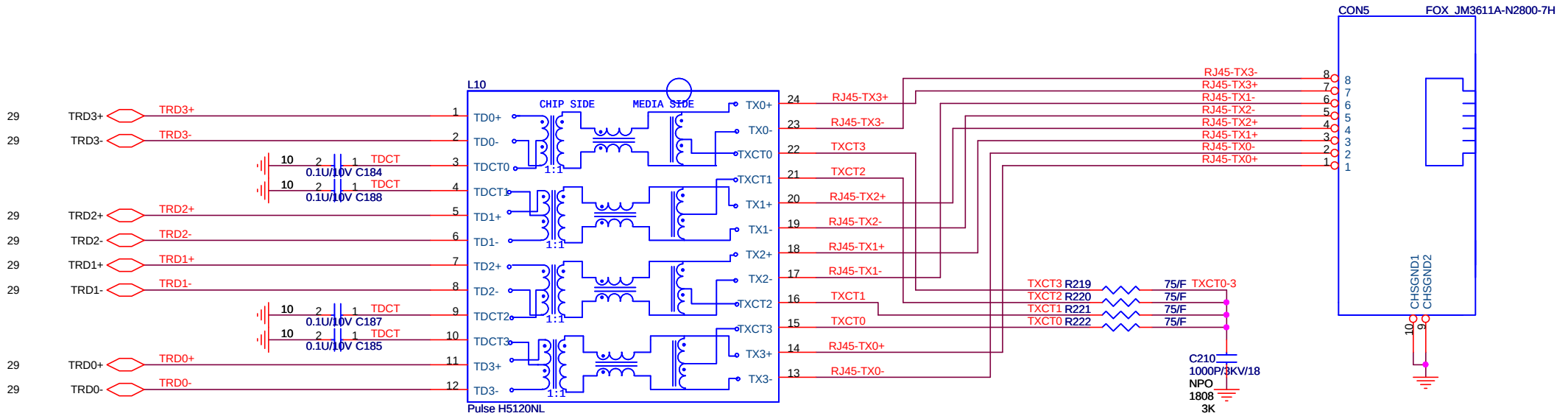

Reserved for EMI.

TRD3+	C191	6.8P/50V
TRD3-	C190	6.8P/50V
TRD2+	C194	6.8P/50V
TRD2-	C195	6.8P/50V
TRD1+	C196	6.8P/50V
TRD1-	C197	6.8P/50V
TRD0+	C192	6.8P/50V
TRD0-	C193	6.8P/50V

LAYOUT NOTE:
CAP CLOSE TO TRANSFORMER
one cap for each pin

QUANTA COMPUTER

Title	LAN SWITCH		
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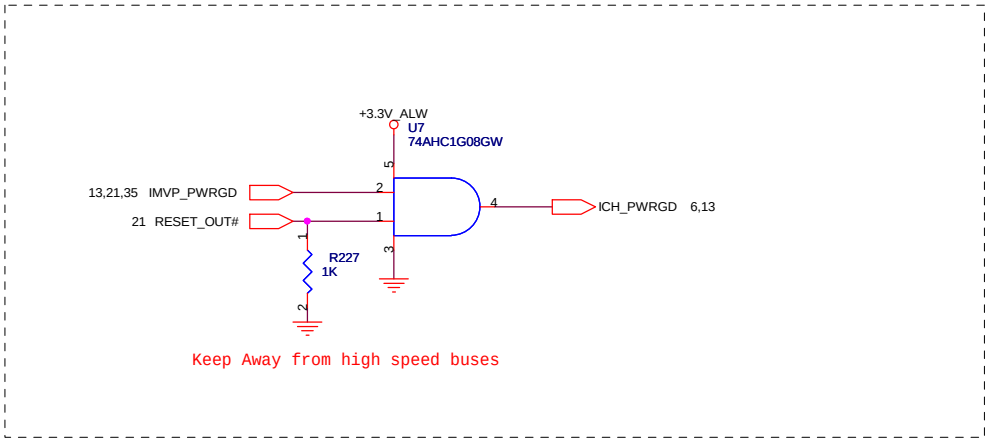

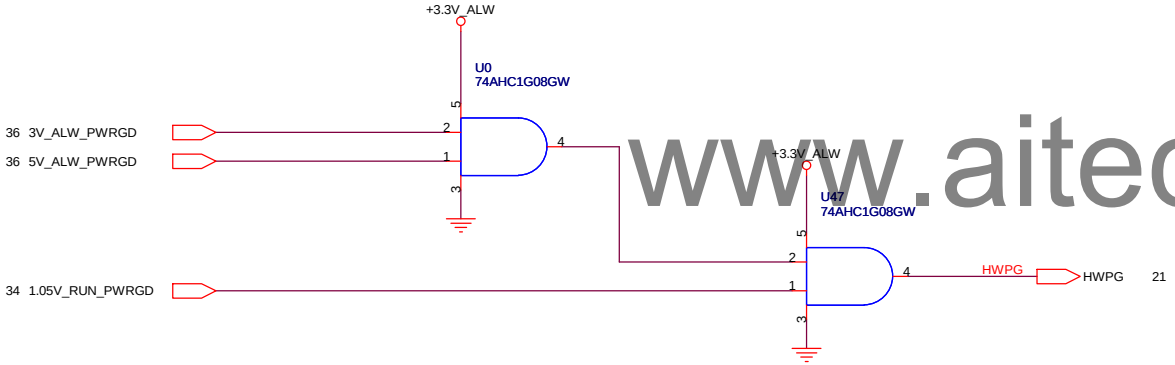

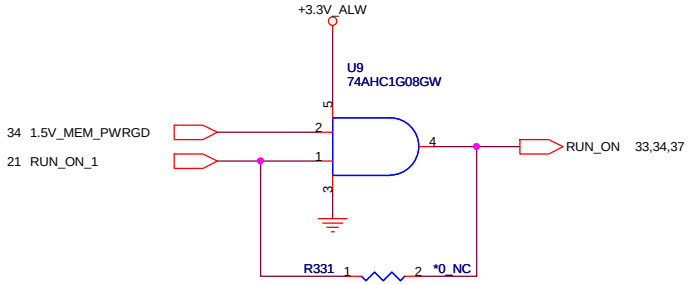

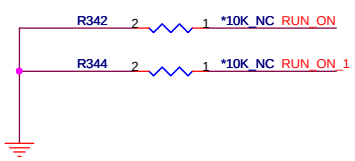

QUANTA COMPUTER

Title	System Reset Circuit	
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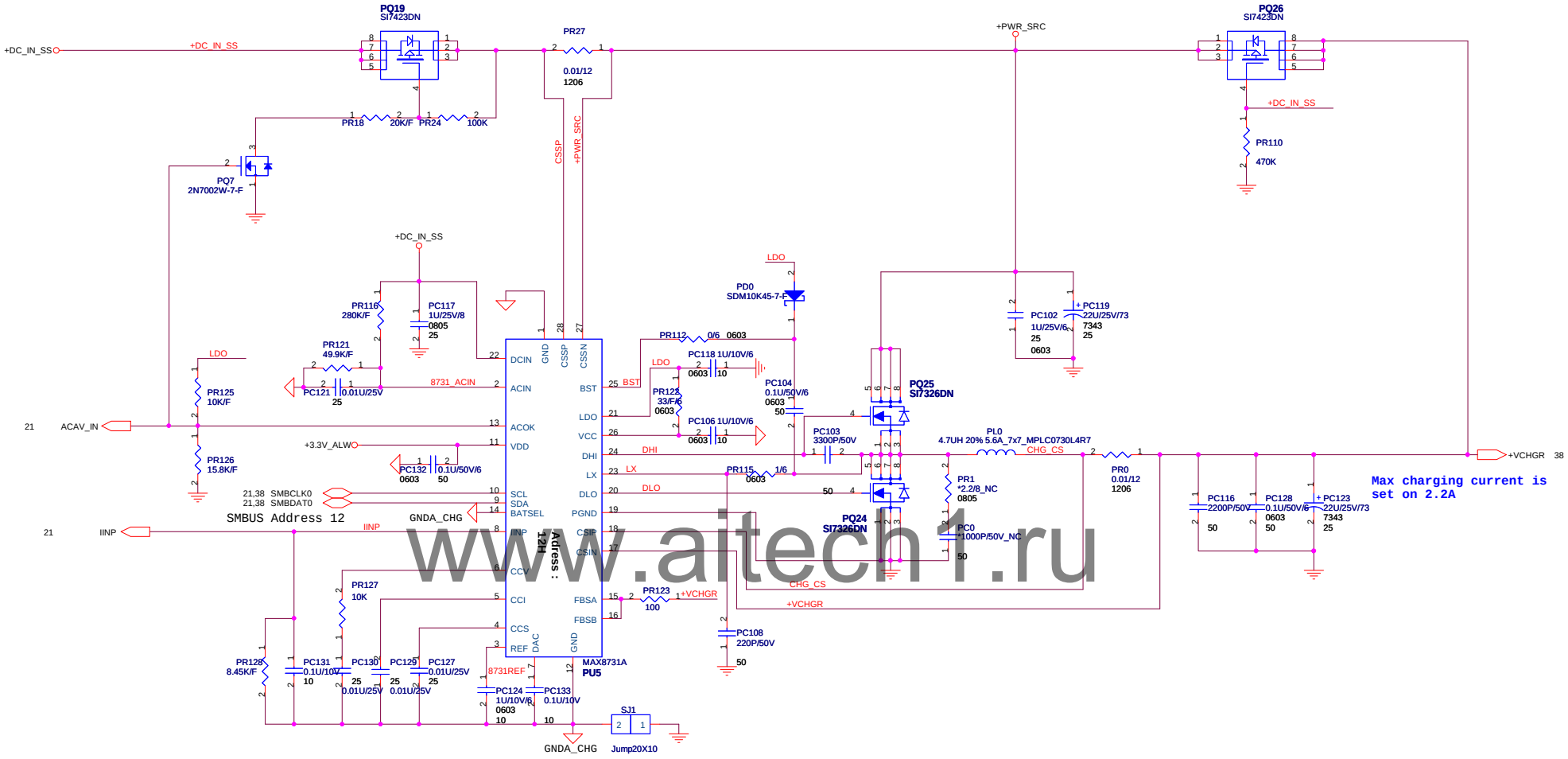

QUANTA COMPUTER

Title	Charger (MAX8731)	
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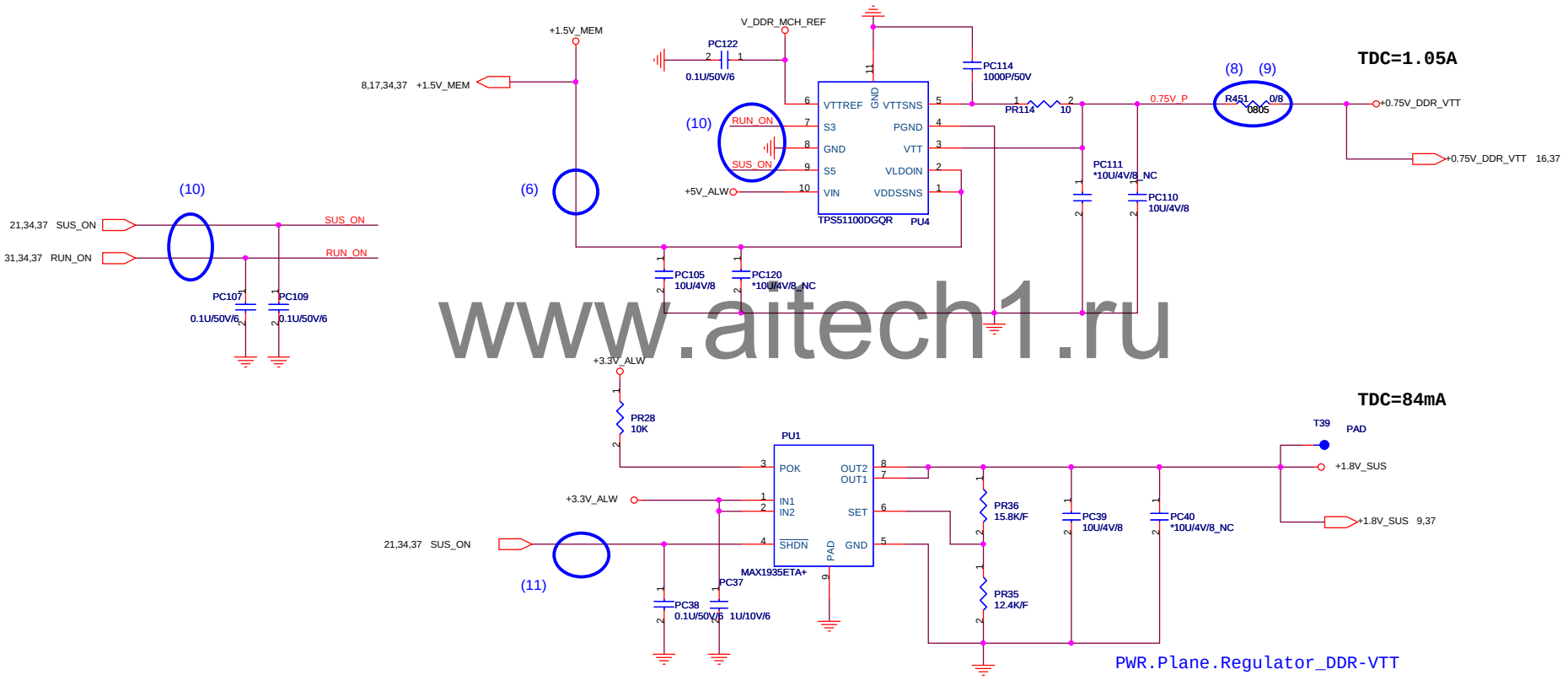

QUANTA COMPUTER

Title	0.75V_DDR_VTT, 1.8V_RUN	
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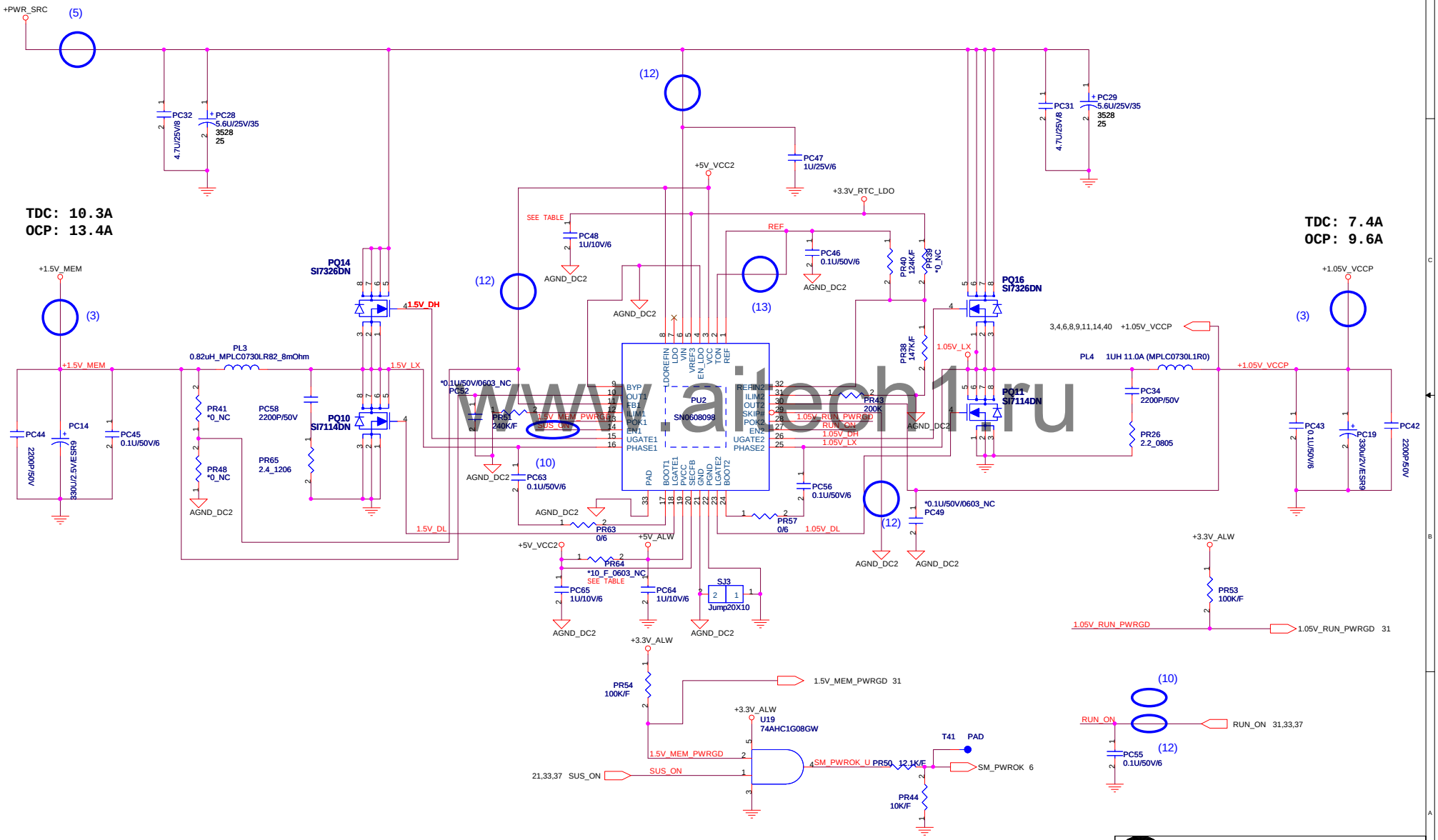
M'09
+1.5V_MEM /+1.05V_VCCP /+3.3_RTC_LDO



REF DESIGNATOR	MAXIM	INTERSIL	TI
PR64	10, 0603	NO STUFF	NO STUFF
PC48	1uF	0.1uF	1uF

QUANTA COMPUTER

Title	1.05V_VCCP & 1.5V_MEM	
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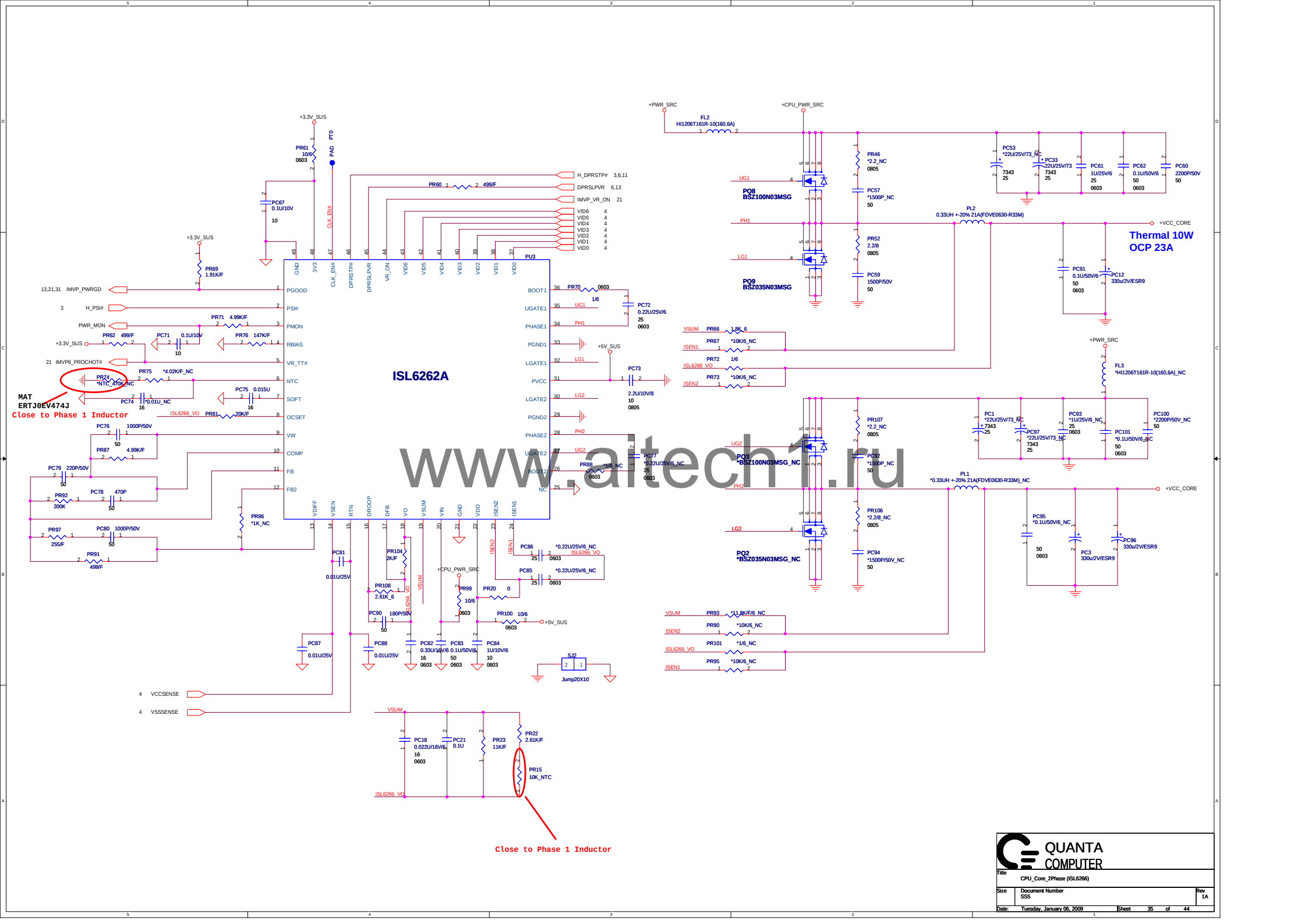


DC/DC +3V_ALW/+5V_SUS/+5V_ALW /+15V_ALW

TDC: 2.5A
OCP: 4A

TDC: 4.3A
OCP: 5.6A

PU0 MAX17020

PQ18 SI7326DN
PQ13 SI7114DN
PQ17 SI7326DN
PQ12 SI7114DN

PR5 390K
PR4 150K/F 0603
PR86 10/6 0603
PR8 *0_NC
PR84 *0_NC
PR11 147K/F
PR14 82K/F
PR21 1/6 0603
PR19 0603
PR82 39K/F
PR77 200K
PR78 *0_NC
PL5 3.3u_6.5A_30mOhm_MPLC0730L3R3
PL6 3.3u_6.5A_30mOhm_MPLC0730L3R3

PC4 1U/25V/6 25 0603
PC25 22U/25V/73 7343 25
PC26 22U/25V/73 7343 25
PC35 1U/25V/6 25 0603
PC5 4.7U/10V/8
PC10 0.1U/10V
PC9 0.1U/50V/6 50 0603
PC8 0.1U/50V/6 50 0603
PC7 1U/10V/6 0603 10
PC22 220U/6.3V/73 7343 6.3
PC13 0.1U/50V/6 0603 50
PC17 0.1U/50V/6 50 0603
PC15 0.1U/50V/6 50 0603
PC16 1U/10V/6 0603 10
PC20 0.1U/50V/6 0603 50
PC23 220U/6.3V/73 6.3 7343
PC68 0.1U/50V/6 50 0603
PC70 0.1U/50V/6 50 0603
PC66 0.1U/50V/6 50 0603
PC69 0.1U/50V/6 50 0603

R182 100K
R194 100K

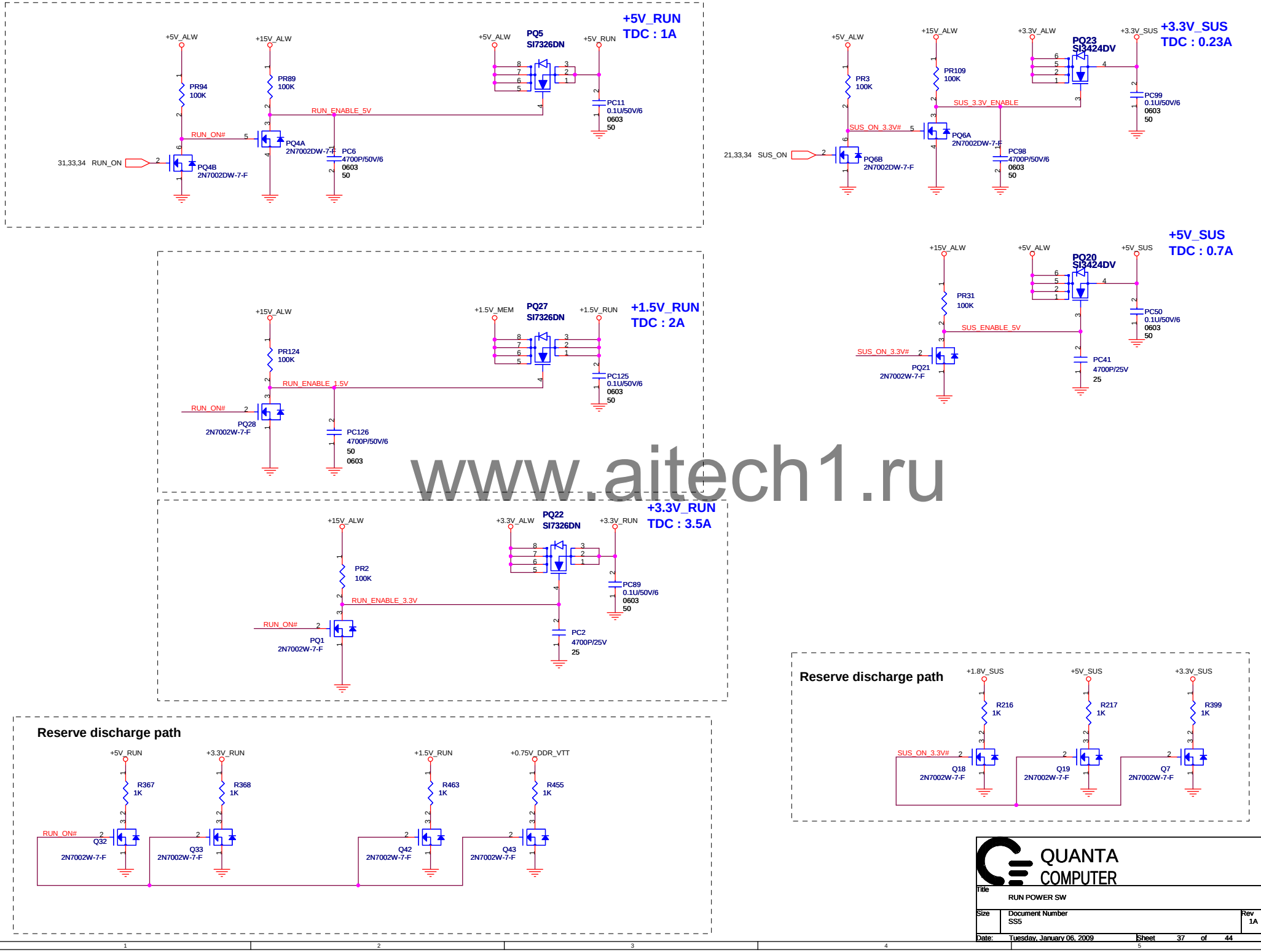
Q12 DDTA114YUA-7-F
Q11 2N7002W-7-F
PD1 BAS316
PD2 BAT54S-7-F
PD3 BAT54S-7-F

SJ4 Jump20X10
SJ5 Jump20X10
SJ6 Jump20X10

+PWR_SRC
+5V_ALW
+5V_ALW2
+3.3V_ALW
+15V_ALW
+5V_DH
+5V_DL
+5V_LX
+3.3V_LX
+3.3V_DH
+3.3V_DL
+5V_EN1
+3.3V_EN2
ISL6237_ONLOD
POK1
POK2
T54 PAD
H_THERMTRIP# 3,6
THERM_STP# 21,26
21 5V_ALW_ON
3V_ALW_PWRGD 31
5V_ALW_PWRGD 31

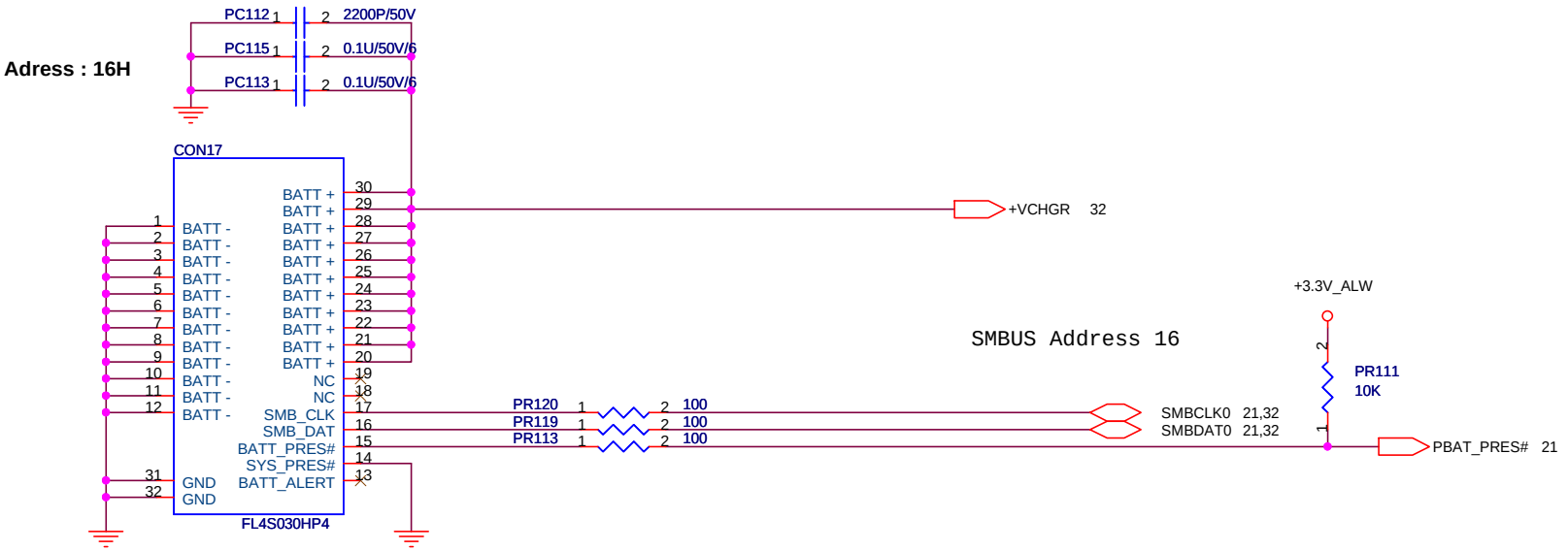
QUANTA COMPUTER

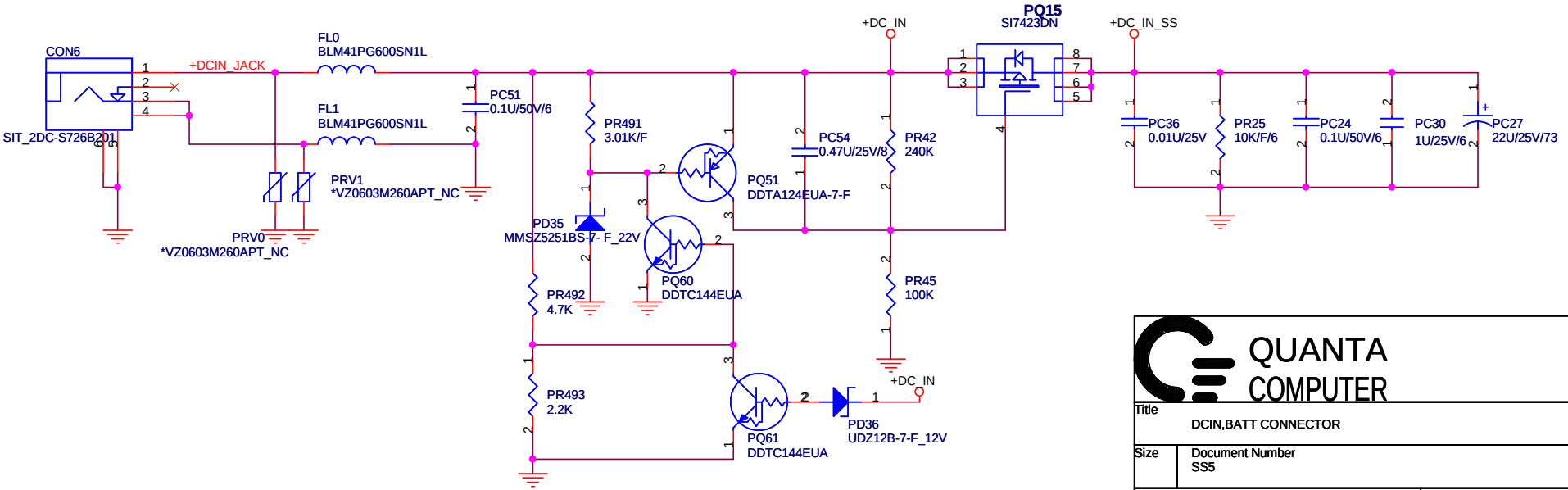
Title	3VALW,5V,3V, Power On	
Size	Document Number SS5	Rev 1A
Date: Tuesday, January 06, 2009	Sheet 36 of 44	



QUANTA COMPUTER

Title	RUN POWER SW	
Size	Document Number SS5	Rev 1A
Date: Tuesday, January 06, 2009	Sheet 37 of 44	

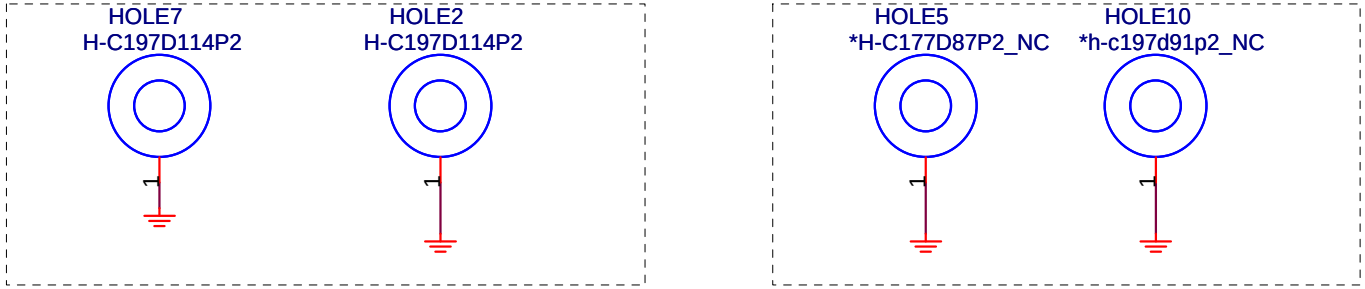




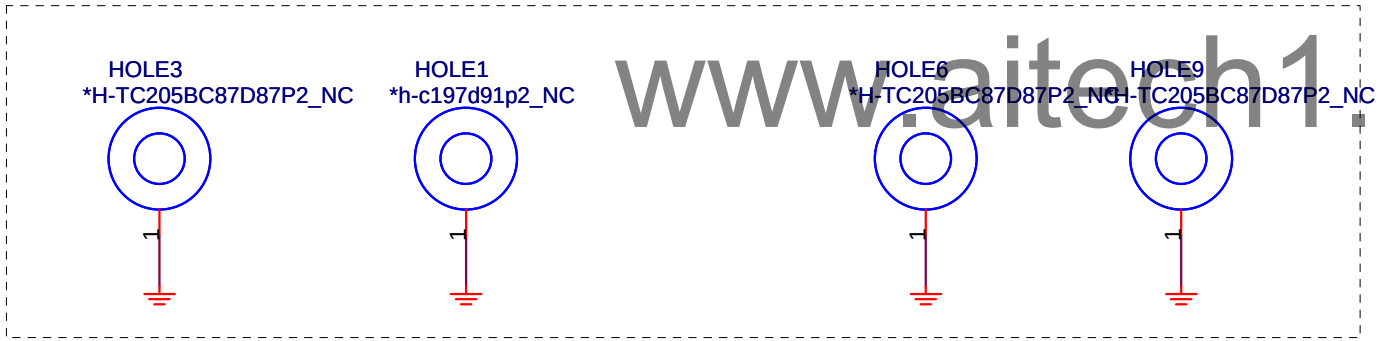
QUANTA COMPUTER

Title	DCIN,BATT CONNECTOR	
Size	Document Number SS5	Rev 1A
Date: Tuesday, January 06, 2009	Sheet 38 of 44	

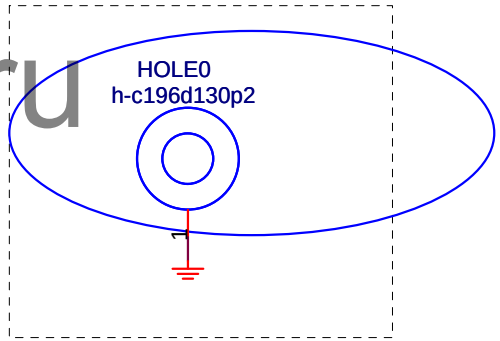
Thermal Screw



Housing Screw



Outer diameter = 4.5mm



P/N is ok.
Also need change FP 12/29.

QUANTA COMPUTER

Title: SCREW PAD		
Size	Document Number: SS5	Rev: 1A
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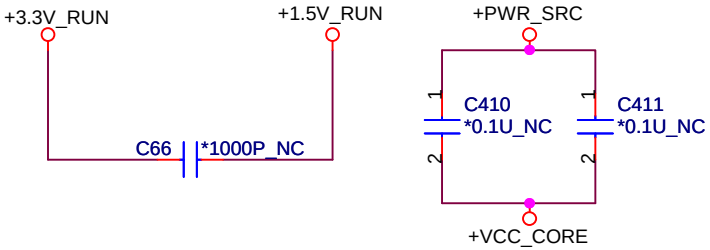
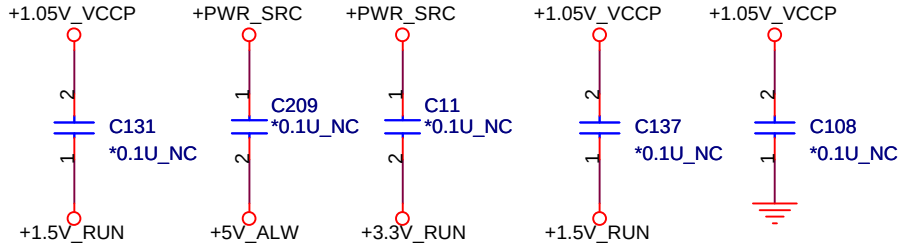
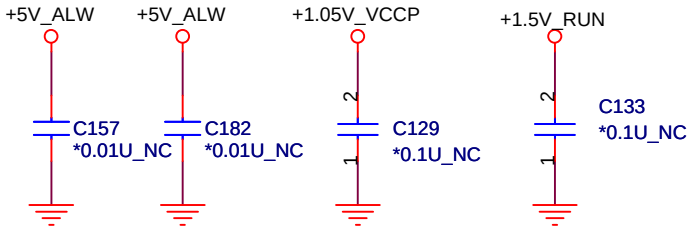
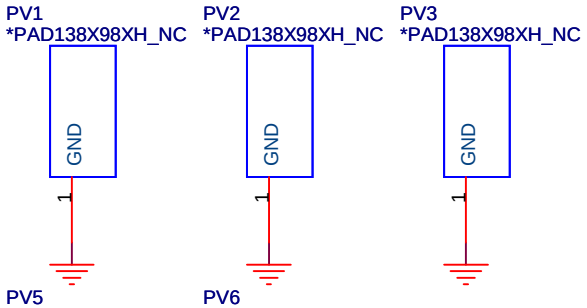
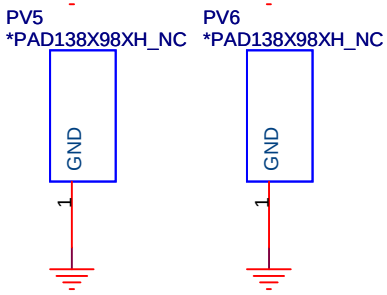
Reserved for EMI. Stitching caps.

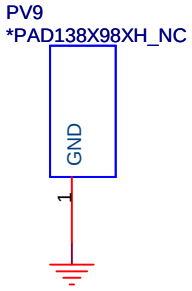






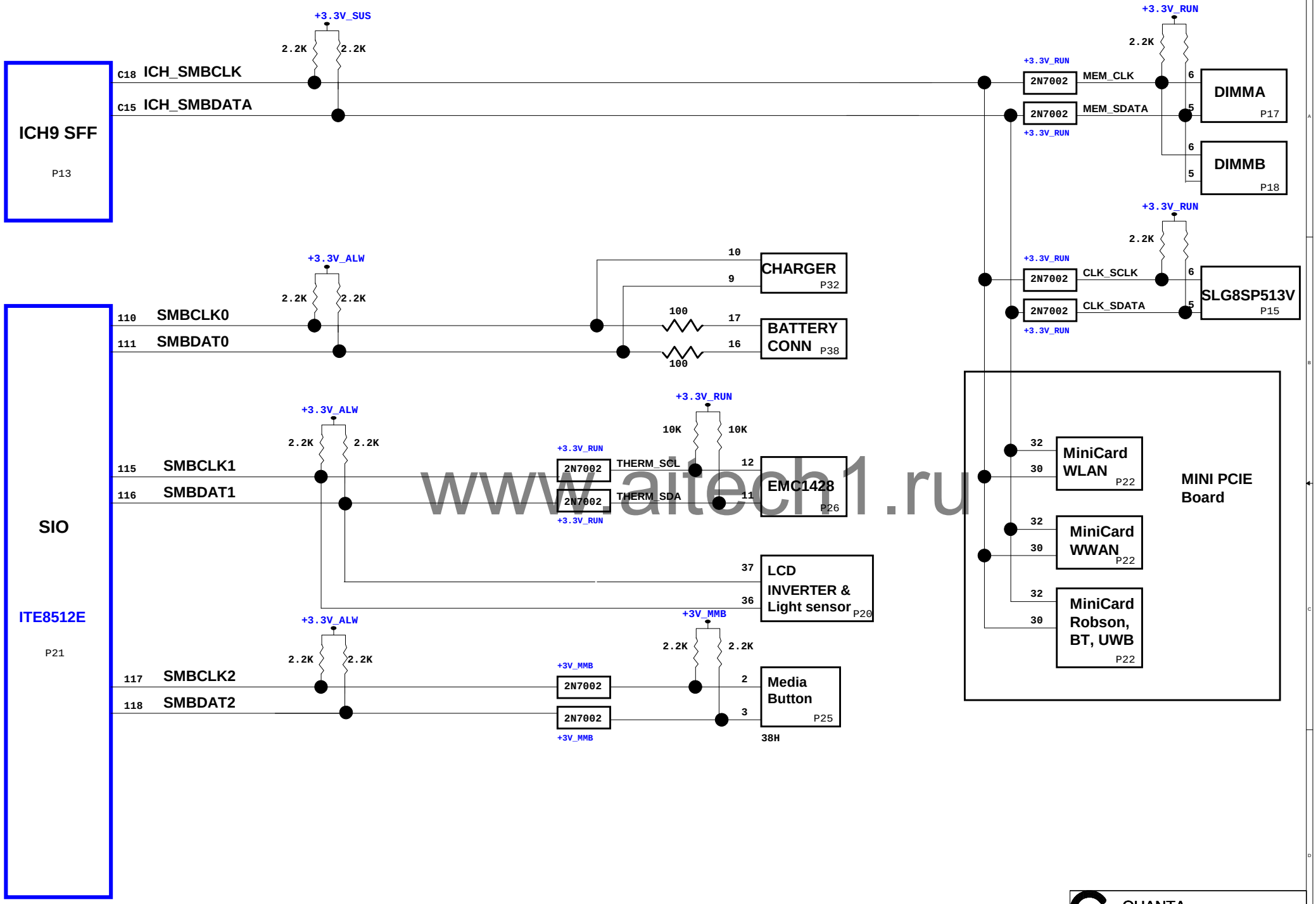






QUANTA COMPUTER

Title	EMI CAP	
Size	Document Number SS5	Rev 1A
Date: Tuesday, January 06, 2009	Sheet 40 of 44	



QUANTA COMPUTER

Title	SMBUS BLOCK	
Size	Document Number FX6	Rev 3A
Date: Tuesday, January 06, 2009	Sheet 41 of 44	

Change List

Item	Page#	Date	T	Issue Description	Solution Description	Rev
				X00 change to X00.1		
1	12	5/20/2008	EE	Schematic have pull up resistor and pull down resistor. Remove all pull up resistor for those signal. SB_WWAN_PCIE_RST#, SB_LOM_PCIE_RST#, SB_WPAN_PCIE_RST#, SB_WLAN_PCIE_RST# and SB_NB_PCIE_RST#.	Depop R361, R133, R72, R407, R74.	X00.1
2	20, 28	5/20/2008	EE	LCD and CCD connect need combin as one connect. Del Camera connect (P28) and change (P20)J1 from 30pin to 44pin. Move 2 USB and 1 Combo connect to MB.	Del CON12(P28) and move rest of Camera componets to P20. Change J1 from 30pin to 44pin.	X00.1
3	23	5/20/2008	EE	Move IO Board connect (2 USB and 1 E-Sata) to Mother Board side.	Add L38, R468, R469, CN1 For USB0 Add L39, R470, R471, CN2 and ESD1 for USB1. Add L40, R472, R473, CON20 for USB2 & E-SATA	X00.1
4	23	5/20/2008	EE	To support USB charger function, Added USB Switch to solve leakage issue.	Added U46 and R474 USB Switch circuit.	X00.1
5	23	5/20/2008	EE	Follow safety design, added Fuse on USB power avoide TPS2062DR no function.	Added PJP9 and FS1_NC for USB0 and USB1. Added PJP10 and FS2_NC for USB3.	X00.1
6	3, 26	5/20/2008	EE	Follow Thermal requirement to measured OTP, CPU, NB, DDR, SB and WWAN temperature.	Added C501, C502, Q48, C503, Q49 for DDR and NB. Added C504, C505, Q50, C506, Q51 for SB and WWAN Added rest of EMC1428 components C508, R477, R475, R476	X00.1
7	12, 23	5/20/2008	EE	For USB P0/P1 use same power rail. Change over current design. Change net OC0# and OC1# to OC0_1#.	Change U17.5 and U17.8 to net OC0_1#. Remove R132.	X00.1
8	25	5/21/2008	EE	Change MMB connect from 15pin to 10pin. Remove Media Buttom function. Added System LED signal on MMB connect.	Change CON11 from 15pin to 10pin. Added SYS_WHITE#_R and SYS_AMBER#_R signal MMB connect.	X00.1
9	28	5/21/2008	EE	Follow ME/ID requirement. Change Audio connect type.	Udate CON2 symbol and footprint.	X00.1
10	38	5/21/2008	EE	Follow ME/ID requirement. Change DC_IN Jack connect type.	Udate CON6 symbol and footprint.	X00.1
11	11	5/23/2008	EE	ME Z-Hing limite, need change RTC type to small size. It need support charge function.	Chnge CON1 footprint and Added R202 1kohm support charge.	X00.1
12	13, 22	5/23/2008	EE	Added USB_MCARD3 detect pin for WWAN card.	Added input port on USSB_MCARD3 and connect to CON15.21	X00.1
13	18	5/23/2008	EE	Memory A and B chanel have same SMBUS address. Change SMBUS address to A4.	Change R147 from pull low to pull up +3.3V_RUN.	X00.1
14	19	5/23/2008	EE	Display Port need chnge to TOP mount type. Change new Connect Footprint.	Change CON7 symbol and Footprint.	X00.1
15	20, 21	5/23/2009	EE	Added SMBUS signal and connection to LCD Connect(J1).	Added SMB_CLK1 form U35.115 to J1.6. SMB_DAT1 from U35.116 to J1.5.	X00.1
16	21, 31	5/23/2009	EE	Remove GPIO diode on GPD0, GPF1 and GPF2.	GPF0 -> SIO_SLP_S3# solve S5 can enter issue. (Remove D0) GPF1 -> IMVP_PWRGD input pin, can't havd diode. (Remove D17) GPF2 -> RESET_OUT# out put pin, don't have leakage concerm. (Remove D7 and R110)	X00.1
17	22, 27	5/23/2009	EE	ME define MIC connect on MB side.Remove MIC signal to 100 pin connect. Change those 2 pin for Thermal Diode signal(WWAN).	REM_DIODE6P_7N -> CON15.98 connection to U43.15 REM_DIODE6N_7P -> CON15.99 connection to U43.14	X00.1
18	22	5/23/2009	EE	ID don't support WLAN/WWAN/WPAN LED. Remove LED signal from CON15. Added 1 pin +5VRUN.	Remove out LED_WWAN#/ LED_BT_UWB# / LED_WLAN_OUT#. CON15-21,56 and 87pin	X00.1
19	23	5/23/2009	EE	Change USB connect layout footprint.	Change CN1 schematic symbol and layout footprint. Change CN2 schematic symbol and layout footprint.	X00.1
20	23	5/23/2009	EE	Change E-Sata/USB connect layout footprint. Added detect# signal for detect USB plug in.	Change CON20 E-Sata/USB connect layout footprint. Connection CON20.14 (USB_COM_DETECT#) to EC.	X00.1
21	24	5/23/2009	EE	Sync with ME and EE keyboard Matrix. Update Footprint.	Update CON19 layout footprint and reserve keyboard pin to match M09 keyboard.	X00.1
22	25	5/23/2009	EE	Power LED and System LED need light during S5. Due to S5 state, +5V-ALW will turn off.	Change R431, U42.5, R393, U33.5, R330, U29.5, R404, U40.5 from +5V_ALW to +5V_ALW2.	X00.1
23	21	5/23/2009	EE	Move Back R233 to MB. Reserved GPIO pull up for EC WUI pin.	Move R233 pull up (+3.3V_ALW) to U35.124 Media_INT#.	X00.1
24	9	5/23/2009	EE	Follow Intel Reference Design. Added AC terminal RC.	Added R479 (0.51ohm) and C502 (22uF) on +1.05M_MPLL	X00.1
25	27	5/23/2009	EE	Add R480 100k on 92HD73C pin 13 SENSEA.	Add R480 100k on 92HD73C pin 13 SENSEA.	X00.1
26	32	5/23/2009	P	Change ACIN threshole to 11.9V from 17V	Change PR116 from 365K/F ohm to 240K/F ohm.	X00.1
27	38	5/23/2009	P	Change to +5V_ALW from +5V_ALW2.	Chanage PR3 pin1 to +5V_ALW from +5V_ALW2.	X00.1
28	38	5/26/2009	P	Change CON17 to FLS030HP1 and update footprint.	Change CON17 footprint to fl4sxxxhp1-30p-r	X00.1
29	38	5/26/2009	EE	Follow layout request to exchange signals.	Exchange CP0, CP2, CP3, CP4, CP5, L18 signals for layout request.	X00.1
30	29	5/28/2009	EE	Follow BCM recommand. Change Pin 27 to correct power rail and add 0.1uF*4 for π type filter.	Change U21.27 to U21.30 and Add C509~C512 at +1.2V_LOM.	X00.1
31	9	5/29/2009	EE	Depop R118 to let VCC_HDA connect to GND.	Depop R118 0 ohm.	X00.1
32	25	5/29/2009		The different power rail between MMB and SIO. Need added level circuit.	Added Q48, Q53, Q52, RP22level shift circuit.	

Change List

Item	Page#	Date	T	Issue Description	Solution Description	Rev
				X00.1 change to X01		
33	32	6/10/2008	EE	Change AC_IN volt threshold on 13.5V with a 280K resister of PR116	Change PR116 from 240K to 280K	X01
34	32	6/11/2008	EE	Change to SI7326 for 2.2A charging	Change PQ24 from SI7114DN to SI7326DN	X01
35	32	6/11/2008	EE	No need to populate them	unpop PR1 and PC0	X01
36	35	6/11/2008	EE	Adjust the slew rate of load line	Chagne PR93 and PR66 from 3.83K to 11.8K Chagne PR104 from 1K to 4.99K, PR108 from 3.83K to 6.49K Chagne PC18 from 0.22u to 0.033u, PC21 from 0.022u to 3300P	X01
37	32-36	6/11/2008	EE	Replace 0R/0603 resister by power jumper	Chagne 0R/0603 to power jumper as the SJ1, SJ2, , SJ3, SJ4	X01
38	32-36	6/11/2008	EE	Replace 0R/0606 resister by short	Replace 0R/0606 resister by short as the PR102, PR103, PR59 , PR68	X01
39	34	6/11/2008	EE	Adjust controller Freq on 400K/300K from 200K/300K	PR32 NC and pop PR33	X01
40	20	6/11/2008	EE	Follow ME define Camera routing. Added Camera connect.	Added CON12 camera connect.	X01
41	19	6/11/2008	EE	DVI monitor can not detected by DVI dongle.	Follow Intel reference Board, added MUX to select I2C or AUX signal.	X01
42	3	6/16/2008	EE	Move CPU ITP Debug test pad to bottom side for ICT engineer requirement.	Added T113, T114, T115, T116 and T117 put on Bottom side.	X01
43	6	6/16/2008	EE	Added NB JTAG Debug test pad on bottom side for ICT engineer requirement.	Added T118, T119, T120 and T121 put on Bottom side.	X01
44	8	6/16/2008	EE	Modify +VDD_GFXCORE power enable pin follow intel CRB design.	Added R485, Q55 and R486.	X01
45	21	6/16/2008	EE	Follow Quanta M09 lesson learn. Connect HD_RST# signal to EC for Mute timing control.	Added ICH_AZ_CODEC_RST# connect to SIO(U35.22)	X01
46	21,24	6/22/2008	EE	Follow MRD design added CAP LED circuit.	ITE8512 (U35.88) GPIO for Cap_LED#. Added R453, R450, Q56, Q59 and R446.	X01
47	24	6/22/2008	EE	Change LED_KB circuit. Change to PWM control.	Modify Q39.	X01
48	31	6/22/2008	EE	Solve Bits issue DF225364, CMOS load defalut when disconnect AC.	Added Pull down on RESET_OUT# to avoid ICH_PWRGD glitch in inital state.	X01
49	3	6/22/2008	EE	H_RESET leakage from pull up resisrtor. Follow Intel remove out it.	Depop R300.	X01
50	3	6/24/2008	EE	+3.3V_RUN faster then H_THERM. H_THERMTRIP will cause +3.3V_ALW shut down.	Change R204 to form 1M to 10M. It will delay Q17 turn on timing.	X01
51	21	6/24/2008	EE	SIO_SLP_S3# have glitch from EC when system power up. Add PD resistor to solve it.	Pull down R487 1k ohm at SIO_SLP_S3#.	X01
52	8	6/24/2008	EE	GFX_VR_EN(0.9V) can't meet 2N7002W-7-F(Vgs=1V~2V). Need change to FDV301N(Vgs=0.85V).	Chagne Q55 from 2N7002W-7-F to FDV301N.	X01
53	29	6/25/2008	EE	Follow Crystal test report. Chagne LAN Crystal caps from 22pF to 33pF.	Chagne C272, C305 from 22pF to 33pF.	X01
54	21	6/25/2008	EE	Reserve PLTRST# option at for U35 pin 20 to detect SIO_A20.	Add R488, R489 to option ICH_PME#, PLTRST#.	X01
55	28	6/25/2008	EE	Follow IDT feedback. Change L3, L5 to BLM18BD601SN1D for AP test.	Change L3, L5 to BLM18BD601SN1D.	X01
56	40	6/25/2008	EE	Follow EMI team feedback. Reserve spring for EMI.	Add PV1~PV10.	X01
57	23	6/25/2008	EE	Follow EMI team feedback. Connect USB connecot dip pin to GND.	Connect CN1, CN2 pin 7, 8 to GND.	X01
58	3	6/26/2008	EE	Reserve R490 1M ohm for Q17 compatiable FDV301V.	Add R490 1M ohm and pull up +V1.05S_CPU.	
				X01 change to X02		
1	27	7/22/2008	EE	Change port F to port A for Microsoft default drive support port A only.	Change port F to port A also swap SENSEA, SENSEB circuit.	X02
2	3,5,6,8,11,13 20,21,28,29,31	8/13/2008	EE	Remove 0 ohm.	Remove R173, R430, R354, R239, R282, R405, R178, R243, R244, R277, R47, R488, R132, R203, R152, R153, R311, R16, R19, R30	X02
3	6,9,13,17,18,21 27,29,34,35	8/14/2008	EE	Remove 0 ohm.	R134, R435, R448, R70, R199, R394, PR58, R161, R319, R260, R261, R353, R357, R313, R329, PR56, R61, R322, R323, R335, R337, R383, R106, R43, PR98	X02
4	23	8/15/2008	EE	Change USB choke to DLP11SN900HL2L for Z-high form 1.6mm to 0.6mm.	Change L38, L39, L40 fp and remove R468, R469, R470, R471, R472, R473.	X02
5	26	8/28/2008	EE	System can't shut down during OTP sest to 85 degree C.Follow SDA to modify OTP to 83 degree C.	Change R477 from 562 ohm to 487 ohm.	X02
6	11	8/29/2008	EE	Confirm Safty team to depop D10 and R136 for RTC charge function.	Depop D10 and R136 10k ohm.	X02
7	35	9/3/2008	EE	Changes for cost down (CPU regulator from two to one phase)	Depop PC53, PR67, PR73, FL3, PC100, PC101, PC93, PC97, PC1, PR107, PC92, PQ3, PQ2, PR106, PC94, PL1, PC95, PC3, PR93, PR90, PR101, PR95, PC77, PR88, PC86, PC85, and PR96 Change PR66 from 11.8K to 1.8K, PR104 from 4.99K to 4.02K, PR108 from 6.49K to 1.8K, PC21 from 3300P to 0.01u, PC18 from 0.033 to 0.068, PR81 from 12.7K to 20K, PR87 from 6.81K to 4.99K, PR91 from 1K to 2K Add a resister of PR20(0R)	X02
8	33, 36, 37	9/3/2008	EE	Changes for cost down	Depop PC25, PC105, PC110, PC39 and PC40 Change PQ23 from SI7326DN to SI3424DV, PQ20 from SI7326DN to SI3424DV, PQ22 from SI7114DN to SI7326DN,	X02

QUANTA COMPUTER

PROJECT : SS5	DOC. NO. : 204	REV: X00	
APPROVED BY : Cory Lin	CHECKED BY: Cory Lin	DRAWN BY : Leo Tseng	DATE : May. 19 , 2008
SHEET 9 OF 11			

Title	Change List1	QUANTA COMPUTER
Size	Document Number SS5	Rev 1A
Date:	Tuesday, January 06, 2009	Sheet 43 of 44

Change List

Item	Page#	Date	T	Issue Description	Solution Description	Rev
9	38	9/3/2008	PR	Reserve a protection circuit to avoid votage variation of input (13<Vin<20)	Add some parts of PR492, Pr493, PR491, PD35, PD36, PQ51, PQ61 and PQ62	X02
10	21	9/4/2008	EE	H/W workaround for DOS re-boot commend.	Depop R489 and Pop R488 0 ohm resistor.	X02
11	6, 8, 20, 21	9/4/2008	EE	Remove R250, R467, R157 0 ohm.	Remove R250, R467, R157 0 ohm.	X02
12	22	9/8/2008	EE	Reserve DMIC DATA/CLK to Minipcie board.	Reserve DMIC DATA/CLK to CON15 pin 56, 93	X02
13	33	9/8/2008	EE	Short PJP6 for thermal module have latch in Power jump.	Remove PJP6 and change +1.8V_RUN_P to +1.8V_SUS.	X02
14	18	9/8/2008	EE	Add C515 for memory +1.5V_MD.	Add C515 for memory +1.5V_MD.	X02
15	23	9/8/2008	EE	To fix USB charge on Blackberry and Ipod in S5 issue.	Change U46 to MAX4983E. Add R491, R492, R493, R494, C516, R495, R496, R497. Remove ESD2.	X02
16	20	9/15/2008	EE	Supply DPST function	Depop R270 and Pop R271 resistor.	X02
17	21	9/15/2008	EE	For cost down ,remove debug LED	Depop R83,R112,R198,LED0,LED1,LED2	X02
				X02 change to X02.1		
18	38	9/18/2008	EE	For Safty to add fuse at battery connector.	Add FS3 at CON17	X02.1
19	6, 21	9/26/2008	EE	Add L_BKLT_EN connect NB's L_BKLT_EN and EC pin 48 to slove LCD can't dispaly issue.	Add L_BKLT_EN connect U6 pin C37 to EC pin 48.	X02.1
20	17, 18	10/02/2008	EE	Follow Intel feedback. Each DRAM device needs to have its own ZQ cal resistor.	Add R498~R505 240 ohm to DRAM U23, U24, U25, U26, U36, U37, U38, U39.	X02.1
21	21	10/07/2008	EE	Change BID from X02 to X02.1	Depop R102, R100, R126 and pop R109, R126, R127 100k ohm.	X02.1
22	13	10/07/2008	EE	Re-add ICH_SMLINK0/1 PU resistor and reserve R260, R261.	Reserve and depop R260, R261 0 ohm and Add RP8 PU resistor for ICH_SMLINK0/1.	X02.1
23	38	10/08/2008	EE	Confimr Power team to remvoe fuse. fuse move on battery.	Rmove FS3 and short by shape.	X02.1
24	33	10/16/2008	PR	rise center voltage from 1.79V to 1.82V	change PR36 from 12.4KF to 15.8KF, and PR35 from 10KF to 12.4K, and pop PC39	X02.1
25	35	10/16/2008	PR	PL2 is not in PSL, so channg it to Toko which is in PSL. And adjust some values for PL2's change.	change PR92 from 97.6K to 200K, PR91 from 2K to 499R, PR104 from 4.02K to 2K, PR108 from 1.8K to 2.61K, PC21 from 0.01uF to 0.1uF, PC18 from 0.068uF to 0.022uF, pop PC3	X02.1
				X02.1 change to A00		
1	27	11/10/2008	EE	Change TPA6040A4 GAIN from 15.6dB to 6dB for speaker midified.	Depop R296 and pop R295 100k ohm.	A00
2	21	11/10/2008	EE	Change Board ID to A00.	Depop R217 and pop R100 10k ohm.	A00
3	3, 34	11/10/2008	EE	Remove PJP0, PJP2 and short by trace for 1.05V, 1.5V.	Remove PJP0, PJP2 and short by trace for 1.05V, 1.5V.	A00
4	36	11/10/2008	EE	Remove PJP1, PJP3 and short by trace for 3.3V, 5V.	Remove PJP1, PJP3 and short by trace for 3.3V, 5V.	A00
5	34, 36	11/10/2008	EE	Remove PJP4, PJP5 and short by trace for +PWR_SRC.	Remove PJP4, PJP5 and short by trace for +PWR_SRC.	A00
6	33	11/10/2008	EE	Remove PJP8 and short by trace. Change PU4.1, PU4.2 to +1.5V_MEM.	Remove PJP8 and short by trace. Change PU4.1, PU4.2 to +1.5V_MEM.	A00
7	36	12/22/2008	EE	Rising up OCP point to cover second source controller IC of PU0	Change PR11 from 110k ohm to 147k ohm.	A00
8	33	12/22/2008	EE	Remove R451 0 ohm and short by trace. Change 0.75V_P to for +0.75V_DDR_VTT.	Remove R451 0 ohm and short by trace. Change 0.75V_P to for +0.75V_DDR_VTT.	A00
9	33	12/29/2008	EE	Remove R451 will effect DDR reference voltage trace.	Restore the R451 0 ohm.	A00
10	33, 34	12/29/2008	P	Remove PR118, PR117 0 ohm and short by trace. Change S5_1.8V to SUS_ON, S3_1.8V to RUN_ON.	Remove PR118, PR117 0 ohm and short by trace. Change S5_1.8V to SUS_ON, S3_1.8V to RUN_ON.	A00
11	33	12/29/2008	P	Remove PR29 0 ohm and short by trace. Remove PR30 *0_NC and NC.	Remove PR29 0 ohm and short by trace. Remove PR30 *0_NC and NC.	A00
12	34	12/29/2008	P	Remove PR34, PR47, PR49, PR55 0 ohm and short by trace. Change EN_2 to RUN_ON.	Remove PR34, PR47, PR49, PR55 0 ohm and short by trace. Change EN_2 to RUN_ON.	A00
13	34	12/29/2008	P	Remove PR33 0 ohm and short by trace. Remove PR32, PR37 *0_NC and NC.	Remove PR33 0 ohm and short by trace. Remove PR32, PR37 *0_NC and NC.	A00
14	36	12/29/2008	P	Remove PR85, PR83, PR12 0 ohm and short by trace. Remove PR10 *0_NC and NC.	Remove PR85, PR83, PR12 0 ohm and short by trace. Remove PR10 *0_NC and NC.	A00
15	36	12/29/2008	P	Remove PR13, PR17 0 ohm and short by trace. Remove PR16 *0_NC and NC.	Remove PR13, PR17 0 ohm and short by trace. Remove PR16 *0_NC and NC.	A00
16	36	12/29/2008	P	Remove PR9 0 ohm and short by trace. Remove PR6, PR7 *0_NC and NC.	Remove PR9 0 ohm and short by trace. Remove PR6, PR7 *0_NC and NC.	A00
17	36	12/29/2008	P	Change PR79, PR80 to short jump SJ5, SJ6.	Change PR79, PR80 to short jump SJ5, SJ6.	A00
18	25	12/29/2008	EE	Change Power/System LED resistor from 220 to 1k ohm to reduce LED brightness.	Change R360 , R382, R366, R442 from 220 to 1k ohm.	A00
19	27	12/29/2008	EE	Follow Dell request. Change TPA6040A4 GAIN from 6dB to 10dB for speaker midified.	Depop R168 and pop R167 100k ohm.	A00
20	9, 14, 27	01/05/2009	EE	Change GMH, ICH, IDT HDA power to 1.5V for slove HDMI no sound issue.	Depop R117 and pop R118 0 ohm. Change U41.3, R101.1 to +1.5V_RUN and R120.1 to +V1.5_MD.	A00
21	21	01/06/2009	EE	HDA bus are +1.5V power rail. The ICH_AZ_CODEC_RST# also need add level shift to connect EC.	Add R506 100k ohm , R507 390k ohm, C135 0.1uF, Q60 3904, Q61 2N7002.	A00

QUANTA COMPUTER

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APPROVED BY : Cory Lin	CHECKED BY: Cory Lin	DRAWN BY : Leo Tseng	DATE : May. 19 , 2008
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